



**CENTAUR™**  
**KS8695PX**  
**Integrated Multi-Port Gateway**  
**Solution**  
  
**Register Description**

**Version 1.01**

**March 2006**

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### **Revision History**

Revision	Date	Summary of Changes
1.0	9/26/03	Initial Release
1.01	3/30/06	EXTACON0, EXTACON1, EXTACON2 Registers corrected.



## 1.0 Overview

### 1.1 Introduction

Micrel's KS8695PX, a member of the **CENTAUR™** line of integrated processors, is a high-performance router-on-a-chip solution for Ethernet and 802.11 a/g/b based embedded systems. Designed for use in communication routers, the KS8695PX integrates a PCI to AHB bridge solution for interfacing with 32-bit PCI, MiniPCI and Cardbus devices. In addition, it also integrates a proven 3<sup>rd</sup> generation 5-port managed switch, an ARM9 RISC processor with MMU, 5 PHY transceivers with corresponding MAC units and Micrel's **XceleRouter** Technology.

The KS8695PX is built around an outstanding CPU core: the 16/32-bit ARM922T RISC processor. The ARM922T is a scalable, high-performance, microprocessor that was developed for integrated system-on-a-chip applications.

The KS8695PX offers configurable 8-Kbyte Instruction Cache and 8-Kbyte Data Cache that reduces the memory access latency for high-performance applications. Its simple, elegant, and fully static design is particularly suitable for cost-effective, power-sensitive applications.

The KS8695PX contains five 10/100 physical layer transceivers (PHY), four for the Local Area Network (LAN), and one for the Wide Area Network (WAN). It also contains the corresponding five Media Access Control (MAC) units with an integrated layer 2 managed switch. The integration of the switch and the analog PHYs make the KS8695PX an extremely cost-effective solution for SOHO router applications because it saves board space and BOM cost. The layer 2 switch contains a 16Kx32 SRAM on-chip memory for frame buffering. The embedded frame buffer memory is designed with a 1.4Gbps on-chip memory bus. This allows the KS8695PX to perform non-blocking frame switching/routing on the fly for many applications.

On the media side, the KS8695PX supports 10BaseT, and 100BaseTX as specified by the IEEE 802.3 committee, as well as 100 Base FX on WAN port and one LAN port.

The KS8695PX supports two modes of operation in the PCI bus environment, Host Bridge Mode, and Guest Bridge Mode. In the Host bridge mode, the ARM9 processor acts as the Host of the entire system. It configures other PCI devices and coordinates their transactions, including initiating transactions between the PCI devices and AHB bus subsystem. An on-chip PCI arbiter is included to determine the PCI bus ownership among PCI master devices.

In Host Bridge Mode, all I/O registers, including those for the embedded switch, can be configured by the ARM922T processor through the on-chip AMBA bus interface. In Guest Bridge Mode, all of the I/O registers can be programmed by either the external Host CPU on the PCI bus, or the local ARM922T host processor through the AMBA bus.

In Guest Bridge mode, the KS8695PX functions as a slave on the PCI bus. The on-chip PCI arbiter is disabled. Either the ARM9 CPU or the PCI Host CPU can configure the KS8695PX subsystem. In either case, the KS8695PX memory subsystem is accessible from either the PCI Host or the ARM9 CPU. Communications between the external Host CPU and the ARM922T can be accomplished through message passing or through shared memory.

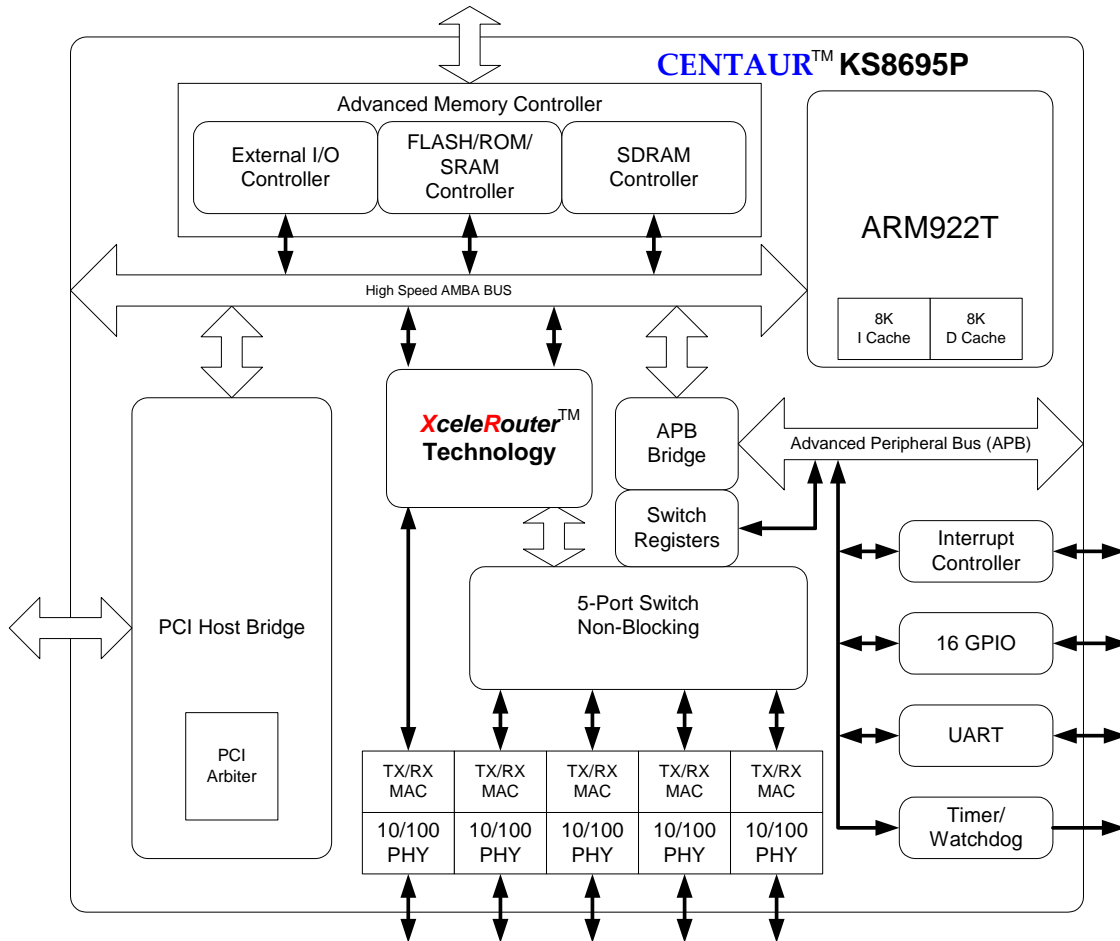




# CENTAUR™ KS8695PX Register Description

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Figure 1 KS8695PX Functional Block Diagram







## **1.2 CPU Features**

- 166MHz ARM922T RISC processor core.
- On-chip AMBA Bus 2.0 interfaces.
- 16-bit Thumb programming to relax memory requirement
- 8-Kbyte Instruction Cache and 8-Kbyte Data Cache
- Little-Endian mode supported.
- Configurable Memory Management Unit
- Supports reduced CPU and System clock speed for power saving

## **1.3 PCI to AHB Bridge Features**

- Support 33MHz, 32-bit DATA PCI Bus.
- Integrated PCI bridge support for interfacing with 32-bit mini-PCI or CardBus devices.
- Independent AHB and PCI Clock speed
- Support 125MHz AHB speed.
- Supports PCI revision 2.1 protocol.
- Supports AHB Bus 2.0 interfaces.
- Supports both regular and memory-mapped I/O on PCI interface.
- Integrated PCI Arbiter with power-on option to enable or disable.
- Supports AHB burst transfers up to 16 data words.
- Configurable PCI registers by Host CPU ARM922T.
- Supports Bus mastership from PCI to AHB or AHB to PCI bus.

## **1.4 Switch Engine**

- 5 port 10/100 Integrated switch with 1 WAN and 4 LAN Physical Layer Transceivers.
- 16Kx32 on-chip SRAM for frame buffering.
- 1.4Gbps on-chip memory bandwidth for wire-speed frame switching.
- 10Mbps, 100Mbps modes of operations for both full and half duplex
- Supports 802.1Q Tag-based VLAN and port-based VLAN
- Supports 802.1p based priority, DiffServ priority and port-based priority.
- Integrated address Look-Up engine, supports 1 K absolute MAC addresses.
- Automatic address learning, address aging and address migration.
- Broadcast storm protection.
- Full duplex IEEE 802.3x flow control.
- Half duplex back pressure flow control.
- Supports IGMP snooping
- Spanning tree protocol support

## **1.5 Advanced Memory Controller Features**

- Supports glueless connection 2 Banks of ROM/SRAM/FLASH memory with programmable 8/16/32 bit data bus and programmable access timing.
- Supports glueless connection to 2 SDRAM Banks with programmable 8/16/32 bit data bus and programmable RAS/CAS latency
- Supports 3 External I/O Banks with programmable 8/16/32 bit data bus and programmable access timing.
- Programmable system clock speed for power management.



### 1.6 Direct Memory Access (DMA) Engines

- Independent MAC DMA engine with programmable burst mode for WAN port.
- Independent MAC DMA engine with programmable burst mode for LAN ports.
- Supports little endian byte ordering for memory buffers and descriptors.
- Contains large independent receive and transmit FIFOs (3KB receive/ 3KB transmit) for back-to-back packet receive, and guaranteed no-underrun packet transmit.
- Data alignment logic and scatter gather capability.

### 1.7 Protocol Engine

- Supports IPv4 IP Header/TCP/UDP Packet checksum generation for host CPU offloading.
- Supports IPv4 Packet filtering based on checksum errors

### 1.8 Network Interface

- Features 5 media access control (MAC) units and 5 physical transceiver units (PHY).
- Supports 10 BaseT, 100 BaseTx on all LAN ports and WAN port. Also supports 100BaseFx on WAN port and one LAN port.
- Supports automatic CRC generation and checking.
- Supports automatic error packet discard.
- Supports IEEE 802.3 Auto-Negotiation algorithm of full-duplex and half-duplex operation for 10Mb/s, 100Mb/s.
- Supports full/half-duplex operation on PHY interfaces.
- Fully compliant with IEEE 802.3 Ethernet standards.
- IEEE 802.3 full-duplex flow control and half-duplex backpressure collision flow control.
- Supports MDI/ MDI-X auto crossover.

### 1.9 Peripherals

- 28 Interrupt sources, including 4 external interrupt sources.
- Normal or fast interrupt mode (IRQ, FIQ) supported.
- Prioritized interrupt handling.
- 16 programmable general purpose I/O. Pins individually configurable to input, output, or I/O mode for dedicated signals.
- 2 programmable 32-bit timers with watchdog timer capability
- High speed UART interface up to 115 kbps.

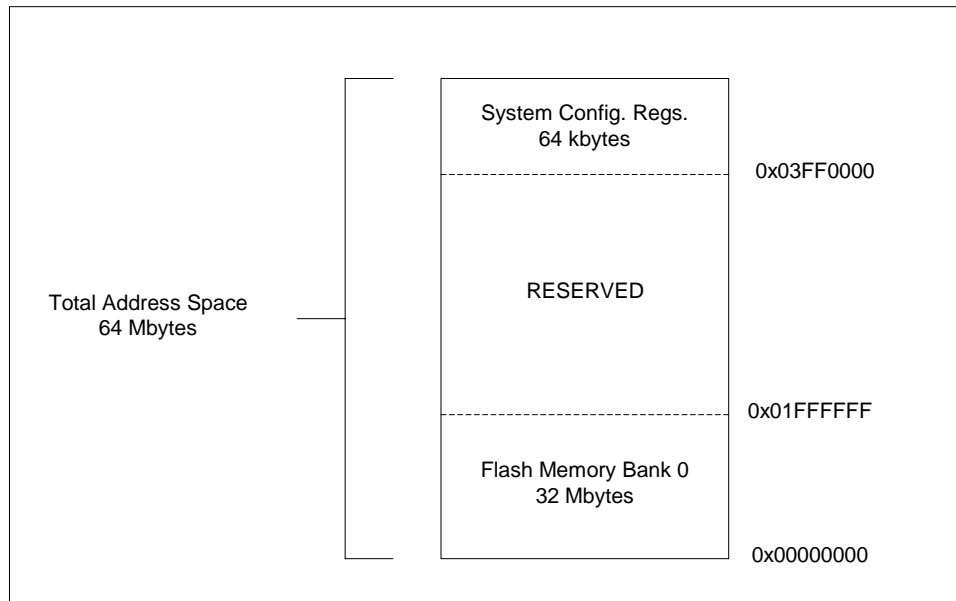
### 1.10 Other Features

- Integrated PLL to generate CPU and system clocks.
- JTAG development interface for ICE connection.
- 19mmx19mm 289 pin PBGA.
- 1.8V CMOS for Core, 3.3V for I/O

## 2.0 Memory Map

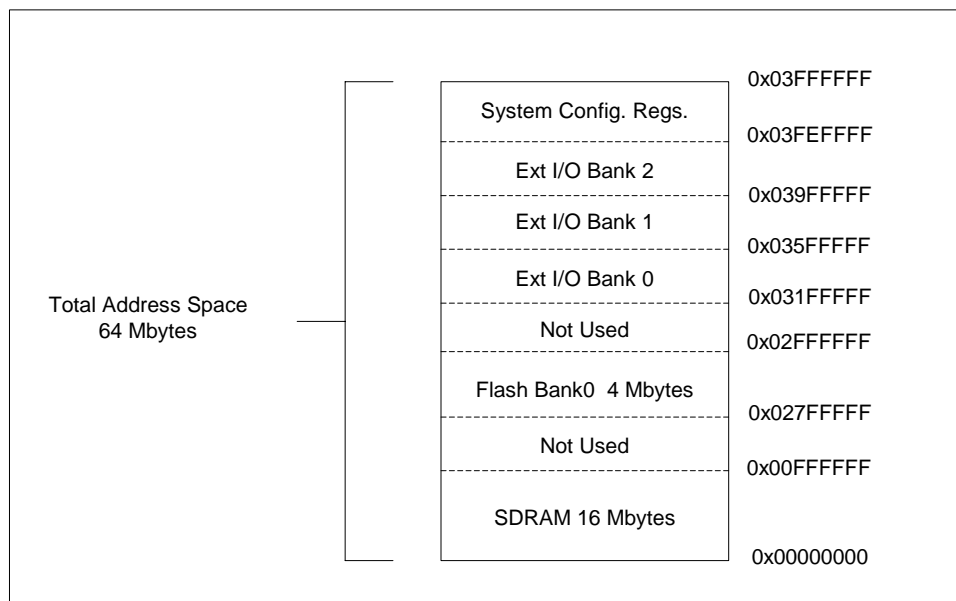
Upon power up, the KS8695PX memory map is configured as shown below.

**Figure 2 KS8695PX Default Memory Map**



The default base address for the the KS8695PX system configuration registers is 0x03ff0000. After power up, the user is free to remap the memory for his/her specific application. Here is an example of the memory space remapped for operation:

**Figure 3 Memory Space Remap Example**

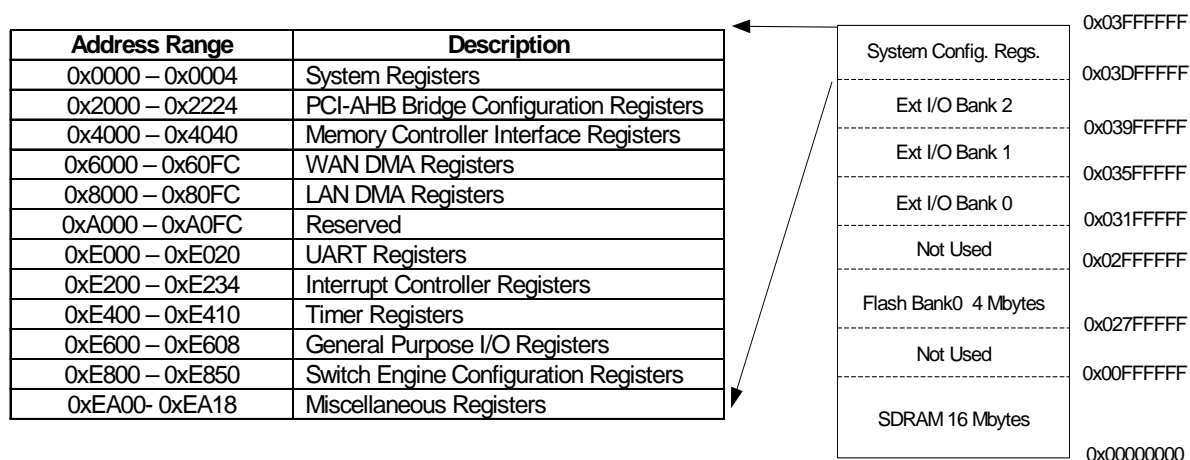




### 3.0 Register Description

The KS8695PX System Configuration Registers (SCR's) are located in a block of 64 kbytes in the host memory address space. After power up and initialization, the user can re-map the SCR's to a desired offset. The SCR's are 32 bits wide. They are 32-bit word aligned and must be accessed using word instructions. A description of the KS8695PX System Configuration Registers follows. The AHB-PCI Bridge configuration registers are also included in the SCR's. A subset of the AHB-PCI Bridge configuration registers are also accessible to an external PCI host when the KS8695PX is configured in PCI guest mode.

**Figure 4 System Configuration Register Mapping**





### 3.1 System Registers

#### 3.1.1 System Configuration Register (SYSCFG Offset 0x0000)

This register determines the start address of all the system control registers. The total system control register space is fixed at a 64Kbyte boundary.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:26	0x00	RO	Reserved
25:16	0x3FF	RW	SPRBP System Configuration Register Bank Base Pointer The Base address of the system configuration register bank. The resolution of the address is 64Kbytes. Note: to place the start address at 1800000H, use the formula: setting value = ( 1800000H / 64K ) << 16.
15:0	0x0	RO	Reserved

#### 3.1.2 System Clock and Bus Control Register (CLKCON Offset 0x0004)

The CLKCON register is written by the CPU to control the internal clock divider for the system clock.

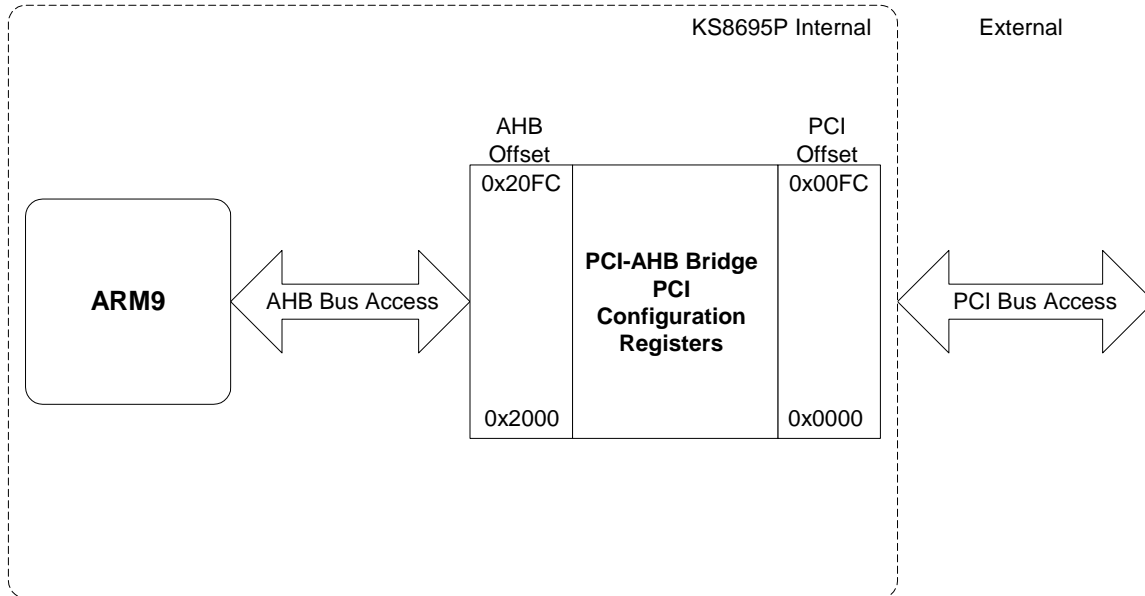
clock

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION																											
31:9	0x0		Reserved																											
8	0	RW	SFMODE System Fast Mode for Simulation This bit is for simulation only. Software should never set this bit.																											
7:3	0x0	RO	Reserved																											
2:0	111	RW	SCDC System Clock Divider Select The internal system clock source is derived from the levels at the CLKSEL and XCLK pins. If CLKSEL is Low, the internal system clock source is the XCLK1 pin. If CLKSEL is High, the internal system clock source is the internal PLL clock synthesizer (5x of XCLK1). The internal system clock is divided by the value of bits 2:0 in this register. The divided clock is used to drive the CPU and system peripherals. If all bits are zero, a non-divided clock is used. The system/CPU clock is selected according to the following table: <table><tr><th></th><th>System Clock</th><th>CPU Clock</th></tr><tr><td>000</td><td>125 MHz</td><td>166 MHz</td></tr><tr><td>001</td><td>100 MHz</td><td></td></tr><tr><td>010</td><td>62.5 MHz</td><td>83 MHz</td></tr><tr><td>011</td><td>50 MHz</td><td></td></tr><tr><td>100</td><td>41.7 MHz</td><td>55.3 MHz</td></tr><tr><td>101</td><td>33.3 MHz</td><td></td></tr><tr><td>110</td><td>31.3 MHz</td><td>41.5 MHz</td></tr><tr><td>111</td><td>25 MHz</td><td></td></tr></table>		System Clock	CPU Clock	000	125 MHz	166 MHz	001	100 MHz		010	62.5 MHz	83 MHz	011	50 MHz		100	41.7 MHz	55.3 MHz	101	33.3 MHz		110	31.3 MHz	41.5 MHz	111	25 MHz	
	System Clock	CPU Clock																												
000	125 MHz	166 MHz																												
001	100 MHz																													
010	62.5 MHz	83 MHz																												
011	50 MHz																													
100	41.7 MHz	55.3 MHz																												
101	33.3 MHz																													
110	31.3 MHz	41.5 MHz																												
111	25 MHz																													

### 3.2 PCI-AHB Bridge Registers (PABCSR)

The PCI-AHB Bridge (PAB) implements all configuration registers required by the PCI specification. These registers are described in the following subsections. Some registers will have two addresses since they can be accessed from both the PCI and AHB buses. The PCI bus configuration register address range is 0x0000-0x00FC, and the AHB bus configuration register address range is 0x2000-0x20FC.

**Figure 5 PCI-AHB Bridge PCI Configuration Register Access**



The PAB enables software-driven initialization and configuration when acting as a host bridge. This allows the software to identify and query the PAB. In the guest bridge mode, the CSID configuration register (subsystem ID and subsystem vendor ID) is programmed by the ARM9, and the remaining configuration registers are programmed by the host system.

The PAB treats configuration space write operations to reserved registers as NO-OPs. That is, the access completes normally on the bus and the data is discarded. Read accesses, to reserved or unimplemented registers, complete normally and a data value of 0 is returned.

Software reset has no effect on the configuration registers. Hardware reset sets the configuration registers to their default values.

The configuration register CSID (subsystem ID and subsystem vendor ID) is programmed by the ARM9 during stage 1 initialization, thus eliminating the need for an EEPROM. Also, Configuration Base Memory Address (CBMA) [3], which is a prefetchable bit, can be initialized in stage 1. Only internal access to these registers is done in stage 1; ie ARM9 accesses do not propagate out to the PCI bus. During stage 2 initialization, the ARM9 programs the remaining configuration registers by generating PCI configuration cycles to the PCI-AHB bridge configuration registers, and the ARM9 programs the system control registers located at offsets 0x2100-0x2224.

The PCI-AHB BRIDGE CSR's (PABCSR's) are located in the host memory address space. The PABCSRs are word aligned, 32 bits long, and must be accessed using word instructions with word-aligned addresses only.

**Note:** Reserved bits should be written with 0. Failing to do so may cause incompatibility issues in a future version of the PCI-AHB BRIDGE. Reserved bits are undefined on read access. Retries on second data transactions occur in response to burst accesses.



## CENTAUR™ KS8695PX Register Description

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PABCSRs are physically located in the KS8695PX. The host uses a single instruction to access a CSR.

The PCI-AHB BRIDGE implements the following configuration and CSR registers. These registers are described below.

**Table 1 Bridge PCI Configuration Registers (PCI Access)**

Configuration Register	Identifier	PCI Bus Address	Default Value
Identification	CFID	0x0000	0x869516C6
Command and status	CFCS	0x0004	0x04400000
Revision	CFRV	0x0008	0x06**0000
Latency Timer	CFLT	0x000C	0x00000000
Configuration Base Memory Address	CBMA	0x0010	0x00000000
Reserved		0x0014-28	0x00000000
Subsystem ID	CSID	0x002C	0x*****
Reserved		0x0030-38	0x00000000
Interrupt	CFIT	0x003C	0x00000100
Reserved		0x0040-FC	0x00000000

**Table 2 Bridge PCI Configuration Registers (AHB Access)**

Register	Identifier	AHB Bus Address	Default Value
Configuration Register: Identification	CRCFID	0x2000	0x869516C6
Configuration Register: Command and status	CRCFCS	0x2004	0x04400000
Configuration Register: Revision	CRCFRV	0x2008	0x06**0000
Configuration Register: Latency Timer	CRCFLT	0x200C	0x00000000
Configuration Register: Configuration Base Memory Address	CRCBMA	0x2010	0x00000000
Reserved		0x2014-28	0x00000000
Configuration Register: Subsystem ID	CRCSID	0x202C	0x*****
Reserved		0x2030-38	0x00000000





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Configuration Register: Interrupt	CRCFIT	0x203C	0x00000100
Reserved		0x2040-FC	0x00000000
PCI-AHB Bridge Configuration Address	PBCA	0x2100	0x00000000
PCI-AHB Bridge Configuration Data	PBCD	0x2104	0x00000000
PCI-AHB Bridge Mode	PBM	0x2200	0x00000000
PAB-AHB Bridge Control and Status	PBCS	0x2204	0x00000000
PCI-AHB Bridge Memory Base Address	PMBA	0x2208	0x00000000
PCI-AHB Bridge Memory Base Address Control	PMBAC	0x220C	0x00000000
PCI-AHB Bridge Memory Base Address Mask	PMBAM	0x2210	0x00000000
PCI-AHB Bridge Memory Base Address Translation	PMBAT	0x2214	0x00000000
PCI-AHB Bridge I/O Base Address	PIOBA	0x2218	0x00000000
PCI-AHB Bridge I/O Base Address Control	PIOBAC	0x221C	0x00000000
PCI-AHB Bridge I/O Base Address Mask	PIOBAM	0x2220	0x00000000
PCI-AHB Bridge I/O Base Address Translation	PIOBAT	0x2224	0x00000000

### 3.2.1 Configuration ID Register (CFID PCI Offset 0x0000)

The CFID register identifies the PCI-AHB BRIDGE.

The following table shows the CFID register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:16	0x8695	RO	Device ID Provides the unique PCI-AHB BRIDGE ID number
15:0	0x16C6	RO	Vendor ID Specifies the manufacturer of the PCI-AHB BRIDGE.

### 3.2.2 Command and Status Configuration Register (CFCS PCI Offset 0x0004)

The CFCS register is divided into two sections: a command register (CFCS[15:0]) and a status register (CFCS[31:16]). The command register provides control of the PCI-AHB BRIDGE's ability to generate and respond to PCI cycles. When 0 is written to this register, the PCI-AHB BRIDGE logically disconnects from the PCI bus for all accesses except configuration accesses.

The status register records status information for PCI bus-related events. **The CFCS status bits are not cleared when they are read. Writing 1 to these bits clears them; writing 0 has no effect.**



## CENTAUR™ KS8695PX Register Description

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The following table describes the CFCS register bit fields.

BIT FIELD	TYPE	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	Status	0	Read/ Clear	Detected Parity Error This bit is set when the bridge detects a parity error, even if parity error handling is disabled (as controlled by bit 6 in the command register).
30	Status	0	Read/ Clear	Signal System Error When set, indicates that the PCI-AHB BRIDGE asserted the system error SERR_N pin.
29	Status	0	Read/ Clear	Received Master Abort When set, indicates that the PCI-AHB BRIDGE terminated a master transaction (except for Special Cycle) with master abort.
28	Status	0	Read/ Clear	Received Target Abort When set, indicates that the PCI-AHB BRIDGE master transaction was terminated due to a target abort.
27	Status	0	Read/ Clear	Generated Target Abort When set, indicates that the PCI-AHB BRIDGE PCI target generated a target abort.
26:25	Status	10	RO	Device Select Timing These bits encode the timing of DEVSEL#. Three allowable timings for assertion of DEVSEL#: 00 – fast 01 – medium 10 – slow
24	Status	0	Read/ Clear	Data Parity Report This bit is set when the following 3 conditions are met: 1) the bus agent asserted PERR# itself (on a read) or observed PERR# asserted (on a write) 2) the PCI-AHB BRIDGE operates as a bus master for the operation that caused the error. 3) the Parity Error Response bit (CFCS[6]) is set.
23:22	reserved	00		Reserved
21	Status	1	RO	66 MHz Capable This read only bit indicates that the PCI-AHB BRIDGE is 66 MHz capable. Its value is always set to 1.
20	Status	0	RO	New Capability New capabilities are not implemented.
19:16	Status	0x0		Reserved
15:10	Command	0x00		Reserved
9	Command	0	RO	Master Fast Back-to-Back Capable Master cannot do fast back-to-back transactions to different devices.
8	Command	0	R/W	System Error Enable Enable bit for SERR# driver. A value of 0 disables the SERR# driver. A value of 1 enables the SERR# driver. This bit's state



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				after RST# is 0. Address parity errors are reported only if this bit and bit 6 are 1.
7	Command	0	RO	Address/Data stepping Bridge does not do address/data stepping.
6	Command	0	RW	Parity Error Response When set, the bridge takes its normal action when a parity error is detected. When the bit is 0, the bridge sets its Detected Parity Error status bit (CFCS[31]) when an error is detected, but does not assert PERR# and continues normal operation. This bit's state after RST# is 0.
5	Command	0	RO	VGA palette access VGA palette snooping is disabled.
4	Command	0	RW	Memory Write and Invalidate Enable When set, the PCI-AHB BRIDGE is allowed to generate the memory write and invalidate command. When reset, the PCI-AHB BRIDGE can only generate memory write command. This bit's state after RST# is 0.
3	Command	0	RO	Special Cycles Response Bridge ignores all special cycle operations.
2	Command	0	RW	Master Operation When set, the PCI-AHB BRIDGE is capable of acting as a bus master. When reset, the PCI-AHB BRIDGE capability to generate PCI accesses is disabled. For normal operation, this bit must be set. This bit's state after RST# is 0.
1	Command	0	RW	Memory Space Access When set, the PCI-AHB BRIDGE responds to memory space accesses. When reset, the PCI-AHB BRIDGE does not respond to memory space accesses. This bit's state after RST# is 0.
0	Command	0	RW	I/O Space Access When set, the PCI-AHB BRIDGE responds to I/O space accesses. When reset, the PCI-AHB BRIDGE does not respond to I/O space accesses. This bit's state after RST# is 0.

### 3.2.3 Configuration Revision Register (CFRV Offset PCI 0x0008)

The CFRV register contains the PCI-AHB BRIDGE revision number.

The following table shows the CFRV register bit fields.

BITS FIELD	Default Value	READ/ WRITE	DESCRIPTION
31:24	0x06	RO	Base Class Indicates device is a bridge, and is equal to 0x06.
23:16	-	RO	Subclass. Host/Guest mode determined by input pin PMBS. 0x00 – In Host bridge mode 0x80 – In Guest bridge mode
15:8	0X00	RO	Reserved
7:4	0x0	RO	Revision Number



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			Indicates the PCI-AHB BRIDGE revision number, and is equal to 0H. This number is incremented for subsequent revision.
3:0	0x0	RO	Step Number Indicates the PCI-AHB BRIDGE step number, and is equal to 0H (chip revision A). This number is incremented for subsequent PCI-AHB BRIDGE steps within the current revision.

#### 3.2.4 Configuration Latency Timer Register (CFLT PCI Offset 0x000C)

This register configures the cache line size field and the latency timer.

The following table shows the CFLT register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:16	0x0000	RO	Reserved
15:8	0x00	R/W	Configuration Latency Timer Specifies, in units of PCI bus clocks, the value of the latency timer of the PCI-AHB BRIDGE. When the PCI-AHB BRIDGE asserts FRAME_N, it enables its latency timer to count. If the PCI-AHB BRIDGE deasserts FRAME_N prior to count expiration, the content of the latency timer is ignored. Otherwise, after the count expires, the PCI-AHB BRIDGE initiates transaction termination as soon as its GNT_N is deasserted.
7:0	0x00	R/W	Cache Line Size Specifies, in unit of 32-bit words(Dword), the system cache line size. The PCI-AHB BRIDGE supports cache line sizes of 4, 8, and 16 Dwords. If an attempt is made to write an unsupported value to this register, the write is ignored and the PCI-AHB BRIDGE does not use the MWI command. If a value other than 4, 8 or 16 is written to the register, the PCI-AHB BRIDGE returns all zeros when the register is read. The driver should use the value of the cache line size to program the cache alignment bits (CSR0[15:14]). The PCI-AHB BRIDGE uses the cache alignment bits for PCI commands that are cache oriented, such as memory-read-line, memory-read-multiple and memory-write-and-invalidate.

#### 3.2.5 Configuration Base Memory Address (CBMA PCI Offset 0x0010)

The CBMA register specify the base memory address for accessing the devices on the AHB. This register must be initialized prior to accessing any AHB device with memory access.

The following table shows the CBMA register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:26	0xFC	R/W	Configuration Base Memory Address Defines the PCI memory base address used to access PAB and AHB resources. The resources reside in a 64MB address range.
25:4	0x0		Reserved.
3	0	RO	Prefetchable 1 – Indicates memory space is prefetchable. 0 – Indicates memory space is not prefetchable.
2:1	00	RO	Type



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			Locate anywhere in 32-bit address space.
0	0	RO	Memory Space Indicator Determines that the register maps into the Memory space. The value in this field is 0.

### 3.2.6 Configuration Base Address (PCI Offsets 0x0014-0x0028)

These configuration base address registers are reserved.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	0x0		Reserved.

### 3.2.7 Subsystem ID Register (CSID PCI Offset 0x002C)

The CSID register is a read-only 32-bit register. The content of the CSID is loaded from the local CPU after a hardware reset. If the CSID is accessed by the PCI host before its content is loaded from the local CPU, the PCI-AHB BRIDGE responds with retry termination on the PCI bus.

The following table shows the CSID register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:16	-	RO	Subsystem ID Indicates a 16-bit field containing the subsystem ID.
15:0	-	RO	Subsystem Vendor ID Indicates a 16-bit field containing the subsystem vendor ID.

The following table shows the access rules of the register.

Category	Description
Value after hardware reset	ARM9 CPU must program the value for Subsystem ID and Subsystem Vendor ID during stage 1 power up configuration.
Write access rules	Only ARM9 CPU can program the Subsystem ID and Subsystem Vendor ID. This register is READ-ONLY on the PCI bus.

### 3.2.8 Configuration Interrupt Register (CFIT PCI Offset 0x003CH)

The CFIT register is divided into two sections: the interrupt line and the interrupt pin. CFIT configures both the system's interrupt and the PCI-AHB BRIDGE interrupt pin connection.

The following table shows the CFIT register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:24	0x00	RO	MAX_LAT This field indicates how often the device needs to gain access to the PCI bus. Time unit is equal to 0.25 us, assuming a PCI clock frequency of 33 MHz. The value after a hardware reset is 00H.
23:16	0x00	RO	MIN_GNT



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			This field indicates the burst period length that the device needs. Time unit is equal to 0.25us, assuming a PCI clock frequency of 33 MHz. The value after a hardware reset is 00H.
15:8	0x01	RO	Interrupt Pin Indicates which interrupt pin that the PCI-AHB BRIDGE uses. The PCI-AHB BRIDGE uses INTA# and the read value is 01H.
7:0	0x00	R/W	Interrupt Line Provides interrupt line routing information. The basic I/O system (BIOS) writes the routing information into to this field when it initialized and configures the system. The value in this field indicates which I of the system interrupt controller is connected to the PCI-AHB BRIDGE's interrupt pin. The driver can use this information to determine priority and vector information. Values in this field are system architecture specific.

### 3.2.9 AHB Internal Access to PCI Configuration Registers (Offsets 0x2000-FC)

The PCI configuration registers can be accessed internally by the ARM9 CPU using the address offsets 0x2000-20FC. They are physically the same registers as the PCI configuration registers, but accessing this address range will not generate PCI configuration cycles on the PCI bus. The only method by which the ARM9 can generate PCI configuration cycles on the PCI bus is through the indirect registers, Configuration Address (PBCA) and Configuration Data (PBCD). During first stage initialization on power-up, the local CPU programs the Subsystem ID and Subsystem Vendor ID configuration registers which are normally programmed by an EEPROM. The following sections describe the PCI configuration registers described earlier with the difference being in the write access of the register bits. All register bits are READ-ONLY except for the Subsystem ID and Subsystem Vendor ID which are READ/WRITE.

#### 3.2.10 Configuration ID Register (CRCFID Offset 0x2000)

The CRCFID register identifies the PCI-AHB BRIDGE.

The following table shows the CRCFID register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:16	0x8695	RO	Device ID Provides the unique PCI-AHB BRIDGE ID number
15:0	0x16C6	RO	Vendor ID Specifies the manufacturer of the PCI-AHB BRIDGE.

#### 3.2.11 Command and Status Configuration Register (CRCFCS PCI Offset 0x2004)

The CRCFCS register is divided into two sections: a command register (CRCFCS[15:0]) and a status register (CRCFCS[31:16]). The command register provides control of the PCI-AHB BRIDGE's ability to generate and respond to PCI cycles.

The status register records status information for the PCI bus-related events. The CRCFCS status bits are not cleared when they are read.

The following table describes the CRCFCS register bit fields.

BIT FIELD	TYPE	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	Status	0	RO	Detected Parity Error This bit is set when the bridge detects a parity error, even if



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				parity error handling is disabled (as controlled by bit 6 in the command register).
30	Status	0	RO	Signal System Error When set, indicates that the PCI-AHB BRIDGE asserted the system error SERR_N pin.
29	Status	0	RO	Received Master Abort When set, indicates that the PCI-AHB BRIDGE terminated a master transaction (except for Special Cycle) with master abort.
28	Status	0	RO	Received Target Abort When set, indicates that the PCI-AHB BRIDGE master transaction was terminated due to a target abort.
27	Status	0	RO	Generated Target Abort When set, indicates that the PCI-AHB BRIDGE PCI target generated a target abort.
26:25	Status	10	RO	Device Select Timing These bits encode the timing of DEVSEL#. Three allowable timings for assertion of DEVSEL#: 00 – fast 01 – medium 10 – slow
24	Status	0	RO	Data Parity Report This bit is set when the following 3 conditions are met: 1) the bus agent asserted PERR# itself (on a read) or observed PERR# asserted (on a write) 2) the PCI-AHB BRIDGE operates as a bus master for the operation that caused the error. 3) the Parity Error Response bit (CRCFCS[6]) is set.
23:22	reserved	00		Reserved
21	Status	1	RO	66 MHz Capable This read only bit indicates that the PCI-AHB BRIDGE is 66 MHz capable. Its value is always set to 1.
20	Status	0	RO	New Capability New capabilities are not implemented.
19:10	Command	0x0		Reserved
9	Command	0	RO	Master Fast Back-to-Back Capable Master cannot do fast back-to-back transactions to different devices.
8	Command	0	RO	System Error Enable Enable bit for SERR# driver. A value of 0 disables the SERR# driver. A value of 1 enables the SERR# driver. This bit's state after RST# is 0. Address parity errors are reported only if this bit and bit 6 are 1.
7	Command	0	RO	Address/Data stepping Bridge does not do address/data stepping.
6	Command	0	RO	Parity Error Response When set, the bridge takes its normal action when a parity error





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				is detected. When the bit is 0, the bridge sets its Detected Parity Error status bit (CFCS[31]) when an error is detected, but does not assert PERR# and continues normal operation. This bit's state after RST# is 0.
5	Command	0	RO	VGA palette access VGA palette snooping is disabled.
4	Command	0	RO	Memory Write and Invalidate Enable When set, the PCI-AHB BRIDGE is allowed to generate the memory write and invalidate command. When reset, the PCI-AHB BRIDGE can only generate memory write command. This bit's state after RST# is 0.
3	Command	0	RO	Special Cycles Response Bridge ignores all special cycle operations.
2	Command	0	RO	Master Operation When set, the PCI-AHB BRIDGE is capable of acting as a bus master. When reset, the PCI-AHB BRIDGE capability to generate PCI accesses is disabled. For normal operation, this bit must be set. This bit's state after RST# is 0.
1	Command	0	RO	Memory Space Access When set, the PCI-AHB BRIDGE responds to memory space accesses. When reset, the PCI-AHB BRIDGE does not respond to memory space accesses. This bit's state after RST# is 0.
0	Command	0	RO	I/O Space Access When set, the PCI-AHB BRIDGE responds to I/O space accesses. When reset, the PCI-AHB BRIDGE does not respond to I/O space accesses. This bit's state after RST# is 0.

#### 3.2.12 Configuration Revision Register (CRCFRV Offset PCI 0x2008)

The CRCFRV register contains the PCI-AHB BRIDGE revision number.

The following table shows the CRCFRV register bit fields.

BIT FIELD	Default Value	READ/ WRITE	DESCRIPTION
31:24	0x06	RO	Base Class Indicates device is a bridge, and is equal to 0x06.
23:16	-	RO	Subclass. Host/Guest mode determined by input pin PBMS. 0x00 – In Host bridge mode 0x80 – In Guest bridge mode
15:8	0X00	RO	Reserved
7:4	0x0	RO	Revision Number Indicates the PCI-AHB BRIDGE revision number, and is equal to 0H. This number is incremented for subsequent revision.
3:0	0x0	RO	Step Number Indicates the PCI-AHB BRIDGE step number, and is equal to 0H (chip revision A). This number is incremented for subsequent PCI-AHB BRIDGE steps within the current revision.



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### 3.2.13 Configuration Latency Timer Register (CRCFLT PCI Offset 0x200C)

This register configures the cache line size field and the latency timer.

The following table shows the CRCFLT register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:16	0x0000	RO	Reserved
15:8	0x00	RO	Configuration Latency Timer Specifies, in units of PCI bus clocks, the value of the latency timer of the PCI-AHB BRIDGE. When the PCI-AHB BRIDGE asserts FRAME_N, it enables its latency timer to count. If the PCI-AHB BRIDGE deasserts FRAME_N prior to count expiration, the content of the latency timer is ignored. Otherwise, after the count expires, the PCI-AHB BRIDGE initiates transaction termination as soon as its GNT_N is deasserted.
7:0	0x00	RO	Cache Line Size Specifies, in unit of 32-bit words(Dword), the system cache line size. The PCI-AHB BRIDGE supports cache line sizes of 4, 8, and 16 Dwords. If an attempt is made to write an unsupported value to this register, the write is ignored and the PCI-AHB BRIDGE does not use the MWI command. If a value other than 4, 8 or 16 is written to the register, the PCI-AHB BRIDGE returns all zeros when the register is read. The driver should use the value of the cache line size to program the cache alignment bits (CSR0[15:14]). The PCI-AHB BRIDGE uses the cache alignment bits for PCI commands that are cache oriented, such as memory-read-line, memory-read-multiple and memory-write-and-invalidate.

### 3.2.14 Configuration Base Memory Address (CRCBMA PCI Offset 0x2010)

The CRCBMA register specify the base memory address for accessing the devices on the AHB.

This register must be initialized prior to accessing any AHB device with memory access.

The following table shows the CRCBMA register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:26	-	RO	Configuration Base Memory Address Defines the PCI memory base address used to access PAB and AHB resources. The resources reside in a 64MB address range. The value read depends on CBMA.
25:4	0x000000		Reserved.
3	0	RW	Prefetchable 1 – Indicates memory space is prefetchable. 0 – Indicates memory space is not prefetchable.
2:1	00	RO	Type Locate anywhere in 32-bit address space.
0	0	RO	Memory Space Indicator Determines that the register maps into the Memory space. The value in this field is 0.



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### 3.2.15 Configuration Base Address (PCI Offsets 0x2014-0x2028)

These configuration base address registers are reserved.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	0x0		Reserved.

### 3.2.16 Subsystem ID Register (CRCSID PCI Offset 0x202C)

The CRCSID register is a read-only 32-bit register. The content of the CRCSID is loaded from the local CPU after a hardware reset. If the CRCSID is accessed by the PCI host before its content is loaded from the local CPU, the PCI-AHB BRIDGE responds with retry termination on the PCI bus.

The following table shows the CRCSID register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:16	0x0	RW	Subsystem ID Indicates a 16-bit field containing the subsystem ID.
15:0	0x0	RW	Subsystem Vendor ID Indicates a 16-bit field containing the subsystem vendor ID.

The following table shows the access rules of the register.

Category	Description
Value after hardware reset	ARM9 CPU must program the value for Subsystem ID and Subsystem Vendor ID during stage 1 power up configuration.
Write access rules	Only ARM9 CPU can program the Subsystem ID and Subsystem Vendor ID. This register is READ-ONLY on the PCI bus.

### 3.2.17 Configuration Interrupt Register (CRCFIT PCI Offset 0x203CH)

The CRCFIT register is divided into two sections: the interrupt line and the interrupt pin. CRCFIT configures both the system's interrupt and the PCI-AHB BRIDGE interrupt pin connection.

The following table shows the CRCFIT register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:24	0x00	RO	MAX_LAT This field indicates how often the device needs to gain access to the PCI bus. Time unit is equal to 0.25 us, assuming a PCI clock frequency of 33 MHz. The value after a hardware reset is 00H.
23:16	0x00	RO	MIN_GNT This field indicates the burst period length that the device needs. Time unit is equal to 0.25us, assuming a PCI clock frequency of 33 MHz. The value after a hardware reset is 00H.
15:8	0x01	RO	Interrupt Pin



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			Indicates which interrupt pin that the PCI-AHB BRIDGE uses. The PCI-AHB BRIDGE uses INTA# and the read value is 01H.
7:0	0x00	RO	<p>Interrupt Line</p> <p>Provides interrupt line routing information. The basic I/O system (BIOS) writes the routing information into to this field when it initialized and configures the system. The value in this field indicates which I of the system interrupt controller is connected to the PCI-AHB BRIDGE's interrupt pin. The driver can use this information to determine priority and vector information. Values in this field are system architecture specific.</p>

#### 3.2.18 PCI-AHB Bridge Configuration Address Register (PBCA Offset 0x2100)

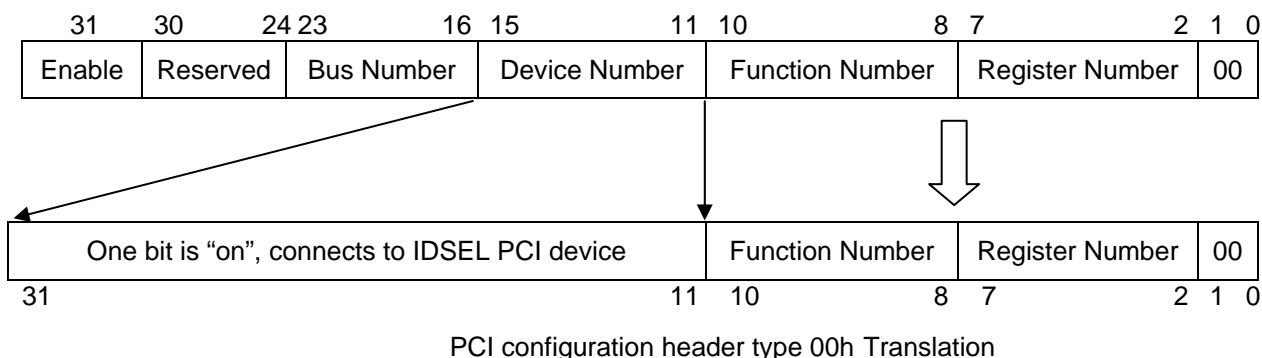
The PBCA register sets the mechanism and address of PCI bus configuration cycle. To start a PCI configuration cycle, write PBCA first then read/write PBCD to complete the transaction.

When initiating a configuration access through PBCA and PBCD, the bridge checks the bus number and device number in PBCA. If the bus number and device number both equal "0", the bridge assumes that its own configuration register is being accessed and the request will not be forwarded to the PCI interface. The bridge will process the configuration access locally.

The following table shows the PBCA register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0	WO	Enable
30:24	0x00	-	Reserved
23:16	0x00	WO	Bus number, indicates whether configuration cycle is on local bus or on another PCI bus segment.
15:11	0x00	WO	Device number, indicates which PCI device is accessed using IDSEL. AD[31:11] are used to connect to IDSEL.
10:8	0x0	WO	Function number
7:2	0x00	WO	Register number, indicates which configuration register is being accessed.
1:0	0x0	WO	Type translation: 00 – PCI configuration cycle Type 00 01 – PCI configuration cycle Type 01

**Figure 6 PCI Type 00 Configuration**





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**Figure 7 PCI Type 01 Configuration**

31	30	24 23	16 15	11 10	8 7	2 1 0
Enable	Reserved	Bus Number	Device Number	Function Number	Register Number	01



31	24 23	16 15	11 10	8 7	2 1 0
Reserved	Bus Number	Device Number	Function Number	Register Number	01

PCI configuration header type 01h Translation

#### 3.2.19 PCI-AHB Bridge Configuration Data Register (PBCD Offset 0x2104)

The PBCD register provides the data interface for the PCI bus configuration cycle. The following table shows the PBCD register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	0x00000000	R/W	PCI configuration register Read/Write data. Read data returned from the PCI configuration read cycle. AHB will be re-tried until the data is available to be read. Write data used in PCI configuration write cycles.

#### 3.2.20 PCI-AHB Bridge Mode Register (PBM Offset 0x2200)

The PBM register sets the PCI-AHB Bridge operating mode. The following table shows the PBM register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	1	RO	PCI-AHB Bridge Function Mode. (READ-ONLY) Selected by static PMBS pin. 1 – Host bridge mode 0 – Guest bridge mode
30:29	00	R/W	PCI-AHB Bridge Bus Mode 00 : PCI Mode 01 : Mini PCI Mode 10 : Card Bus Mode 11 : Reserved
28:0	0x0	RO	Reserved

#### 3.2.21 PCI-AHB Bridge Control and Status Register (PBCS Offset 0x2204)

The control register contains all the control bits for the PCI-AHB BRIDGE. In Host Bridge mode, PBCS indicates to the ARM when configuration cycles can be generated on the PCI bus. In Guest Bridge mode the PBCS register is read by the PCI host to determine when the bridge can be accessed.



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The following table shows the PBCS register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0	RW	SWR Software Reset When set, the PCI-AHB BRIDGE resets all internal hardware with the exception of the PCI configuration area.
30:29	00	RW	Prefetch Limit Allows the user to control the amount of data to be read by a PCI-to-AHB burst read. During PCI burst read with linear increment mode, the bridge prefetch data from the AHB bus up to the Prefetch Limit boundary. During PCI burst read with cache line wrap mode, the bridge prefetch data from the AHB bus up to the smaller value of Prefetch Limit boundary or the cacheline size boundary in the PCI configuration register. The encoding is as follows: 00 : Prefetch limit equals 4 words 01 : Prefetch limit equals 8 words 10 : Prefetch limit equals 16 words 11 : Reserved
28	1	RW	PCI Configuration External Access Disable 1 : Force retry response to PCI configuration cycles. Effectively disables PCI configuration register access on the PCI bus. 0 : The bridge will respond to PCI configuration cycles directed to it from an external PCI device.
28:0	0x0	RO	Reserved

### 3.2.22 PCI-AHB Bridge Memory Base Address Register (PMBA Offset 0x2208)

The PMBA register defines the AHB address range used to generate memory mapped cycles on the PCI bus.

The following table shows the PMBA register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:12	0x6000_0	RW	PCI memory mapped base address. For downstream accesses, this is the start of the AHB address range (range is determined by PMBAM) that will generate memory mapped cycles on the PCI bus. Note the following address ranges are offlimits: 0x0 – 0x03FF_FFFF 0x4000_0000 – 0x5FFF_FFFF 0xC000_0000 – 0xDFFF_FFFF
11:0	0x000	RO	Reserved.

### 3.2.23 PCI-AHB Bridge Memory Base Address Control Register (PMBAC Offset 0x220C)

The PMBAC register is used for address translation control.

The following table shows the PMBAC register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0	RW	Address Translation Enable If this bit is set, downstream address translation for the memory mapped range is enabled.



## CENTAUR™ KS8695PX Register Description

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30:0	0x0000	RO	Reserved
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### 3.2.24 PCI-AHB Bridge Memory Base Address Mask (PMBAM Offset 0x2210)

The PMBAM register specifies address masking for memory mapped cycles on the PCI bus.

The following table shows the PMBAM register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:12	0xFC00_0	RW	Address Unmask. For each bit: 1 – don't mask the address bit 0 – mask the address bit Note: all the don't mask bits must be contiguous. Also, this determines the address range (masked address bits) for downstream memory mapped operations.
11:0	0x000	RO	Because the minimum block size is 4 KB, this field is always 0x000 (the 12 lower address lines are never compared with the PMBA register value).

### 3.2.25 PCI-AHB Bridge Memory Base Address Translation (PMBAT Offset 0x2214)

The PMBAT register specifies the address translation for PCI memory mapped bus cycles.

The following table shows the PMBAT register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:12	-	RW	Translation Address This register value is used when address translation is enabled. Each value on address lines not masked by PMBAM register setting is replaced by the corresponding bit value of the PMBAT register for PCI bus accesses.
11:0	0x000	RO	Because the minimum block size is 4 KB, this field is always 0x000 (the 12 lower address lines are never compared with the PMBA register value).

### 3.2.26 PCI-AHB Bridge I/O Base Address Register (PIOBA Offset 0x2218)

The PIOBA register defines the AHB address range used to generate I/O mapped cycles on the PCI bus.

The following table shows the PIOBA register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:12	0x8000_0	RW	PCI I/O mapped base address. For downstream accesses, this is the start of the AHB address range (range is determined by PIOBAM) that will generate I/O cycles on the PCI bus. Note the following address ranges are offlimits: 0x0 – 0x03FF_FFFF 0x4000_0000 – 0x5FFF_FFFF 0xC000_0000 – 0xDFFF_FFFF
11:0	0x000	RO	Reserved.





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### 3.2.27 PCI-AHB Bridge I/O Base Address Control Register (PIOBAC Offset 0x221C)

The PIOBAC register is used for address translation control.  
The following table shows the PIOBAC register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0	RW	Address Translation Enable If this bit is set, downstream address translation for the I/O mapped range is enabled.
30:0	0x0	RO	Reserved

### 3.2.28 PCI-AHB Bridge I/O Base Address Mask (PIOBAM Offset 0x2220)

The PIOBAM register specifies address masking for PCI I/O mapped cycles.  
The following table shows the PIOBAM register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:12	0xFC00_0	RW	Address Unmask. For each bit: 1 – don't mask the address bit 0 – mask the address bit Note: all the don't mask bits must be contiguous. Also, this determines the address range (masked address bits) for downstream I/O mapped operations.
11:0	0x000	RO	Because the minimum block size is 4 KB, this field is always 0x000 (the 12 lower address lines are never compared with the PIOBAM register value).

### 3.2.29 PCI-AHB Bridge I/O Base Address Translation (PIOBAT Offset 0x2224)

The PIOBAT register specifies the address translation for PCI I/O mapped bus cycles.  
The following table shows the PIOBAT register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:12	-	RW	Translation Address This register value is used when address translation is enabled. Each value on address lines not masked by PIOBAM register setting is replaced by the corresponding bit value of the PIOBAT register for PCI bus accesses.
11:0	0x000	RO	Because the minimum block size is 4 KB, this field is always 0x000 (the 12 lower address lines are never compared with the PIOBAT register value).



### 3.3 Memory Controller

#### 3.3.1 External I/O Access Control Register 0(EXTACON0 Offset 0x4000)

The system has three external I/O access control registers that control external I/O banks. These registers correspond to the three external I/O banks that are supported by the KS8695PX. External I/O access cycles are controlled through EXTACON0, EXTACON1, EXTACON2, or through an external wait signal, EWAITN. The delay times of the control signals (OEN, WBEN, ECSN) can be programmed to obtain access cycles that are longer than those possible with a specified value.

The following table shows the EXTACON0 register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:22	-	RW	EB0NPTR External I/O Bank 0 Last Address Pointer This value is the current bank end address. The last address is calculated as {EB0NPTR, 0xffff}.
21:12	-	RW	EB0BPTR External I/O Bank 0 Base Pointer This value is the start address of the External I/O Bank 1. The start address is calculated as EB0BPTR << 16.
11:9	-	RW	EB0TACT External I/O Bank 0 Write Enable/Output Enable Active Time The access time for Bank 0 is defined in units of system clock cycles. TMULT = 0 000 = 1 cycle 001 = TMULT + 2 cycles 010 = 2 x TMULT + 3 cycles 011 = 3 x TMULT + 4 cycles 100 = 4 x TMULT + 5 cycles 101 = 5 x TMULT + 6 cycles 110 = 6 x TMULT + 7 cycles 111 = 7 x TMULT + 8 cycles  TMULT > 0 000 = 2 <sup>TMULT</sup> + 3 cycles 001 = 1 x 2 <sup>TMULT</sup> + 2 <sup>TMULT</sup> + 3 cycles 010 = 2 x 2 <sup>TMULT</sup> + 2 <sup>TMULT</sup> + 3 cycles 011 = 3 x 2 <sup>TMULT</sup> + 2 <sup>TMULT</sup> + 3 cycles 100 = 4 x 2 <sup>TMULT</sup> + 2 <sup>TMULT</sup> + 3 cycles 101 = 5 x 2 <sup>TMULT</sup> + 2 <sup>TMULT</sup> + 3 cycles 110 = 6 x 2 <sup>TMULT</sup> + 2 <sup>TMULT</sup> + 3 cycles 111 = 7 x 2 <sup>TMULT</sup> + 2 <sup>TMULT</sup> + 3 cycles Note: Please see section 3.3.6 for TMULT definition.
8:6	-	RW	EB0TCOH External I/O Bank 0 Chip Select Hold Time The Chip Select Hold time for Bank 0 is defined in units of system clocks. 000 = 1 cycle 001 = TMULT + 2 cycles



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			010 = 2 x TMULT + 3 cycles 011 = 3 x TMULT + 4 cycles 100 = 4 x TMULT + 5 cycles 101 = 5 x TMULT + 6 cycles 110 = 6 x TMULT + 7 cycles 111 = 7 x TMULT + 8 cycles
5:3	-	RW	EB0TACS External I/O Bank 0 Address Setup Time before ECSN The address setup time for Bank 0 is defined in units of system clocks. 000 = 0 cycle 001 = TMULT + 1 cycles 010 = 2 x TMULT + 2 cycles 011 = 3 x TMULT + 3 cycles 100 = 4 x TMULT + 4 cycles 101 = 5 x TMULT + 5 cycles 110 = 6 x TMULT + 6 cycles 111 = 7 x TMULT + 7 cycles
2:0	-	RW	EB0TCOS External I/O Bank 0 Chip Select Setup Time before OEN The chip select setup time for Bank 0 is defined in units of system clocks. 000 = 1 cycle 001 = TMULT + 2 cycles 010 = 2 x TMULT + 3 cycles 011 = 3 x TMULT + 4 cycles 100 = 4 x TMULT + 5 cycles 101 = 5 x TMULT + 6 cycles 110 = 6 x TMULT + 7 cycles 111 = 7 x TMULT + 8 cycles

### 3.3.2 External I/O Access Control Register 1(EXTACON1 Offset 0x4004)

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:22	-	RW	EB1NPTR External I/O Bank 1 Last Address Pointer This value is the current bank end address. The last address is calculated as {EB1NPTR, 0xffff}.
21:12	-	RW	EB1BPTR External I/O Bank 1 Base Pointer This value is the start address of the External I/O Bank 1. The start address is calculated as EB1BPTR << 16.
11:9	-	RW	EB1TACT External I/O Bank 1 Write Enable/Output Enable Active Time The access time for Bank 1 is defined in units of system clocks. TMULT = 0 000 = 1 cycle 001 = TMULT + 2 cycles 010 = 2 x TMULT + 3 cycles 011 = 3 x TMULT + 4 cycles



# CENTAUR™ KS8695PX Register Description

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			<p>100 = 4 x TMULT + 5 cycles  101 = 5 x TMULT + 6 cycles  110 = 6 x TMULT + 7 cycles  111 = 7 x TMULT + 8 cycles</p> <p>TMULT &gt; 0  000 = 2<sup>TMULT</sup> + 3 cycles  001 = 1 x 2<sup>TMULT</sup> + 2<sup>TMULT</sup> + 3 cycles  010 = 2 x 2<sup>TMULT</sup> + 2<sup>TMULT</sup> + 3 cycles  011 = 3 x 2<sup>TMULT</sup> + 2<sup>TMULT</sup> + 3 cycles  100 = 4 x 2<sup>TMULT</sup> + 2<sup>TMULT</sup> + 3 cycles  101 = 5 x 2<sup>TMULT</sup> + 2<sup>TMULT</sup> + 3 cycles  110 = 6 x 2<sup>TMULT</sup> + 2<sup>TMULT</sup> + 3 cycles  111 = 7 x 2<sup>TMULT</sup> + 2<sup>TMULT</sup> + 3 cycles</p>
8:6	-	RW	<p>EB1TCOH External I/O Bank 1 Chip Select Hold Time  The Chip Select Hold time for Bank 1 is defined in units of system clocks.  000 = 1 cycle  001 = TMULT + 2 cycles  010 = 2 x TMULT + 3 cycles  011 = 3 x TMULT + 4 cycles  100 = 4 x TMULT + 5 cycles  101 = 5 x TMULT + 6 cycles  110 = 6 x TMULT + 7 cycles  111 = 7 x TMULT + 8 cycles</p>
5:3	-	RW	<p>EB1TACS External I/O Bank 1 Address Setup Time before ECSN  The address setup time for Bank 1 is defined in units of system clock.  000 = 0 cycle  001 = TMULT + 1 cycles  010 = 2 x TMULT + 2 cycles  011 = 3 x TMULT + 3 cycles  100 = 4 x TMULT + 4 cycles  101 = 5 x TMULT + 5 cycles  110 = 6 x TMULT + 6 cycles  111 = 7 x TMULT + 7 cycles</p>
2:0	-	RW	<p>EB1TCOS External I/O Bank 1 Chip Select Setup Time before OEN  The chip select setup time for Bank 1 is defined in units of system clock.  000 = 1 cycle  001 = TMULT + 2 cycles  010 = 2 x TMULT + 3 cycles  011 = 3 x TMULT + 4 cycles  100 = 4 x TMULT + 5 cycles  101 = 5 x TMULT + 6 cycles  110 = 6 x TMULT + 7 cycles</p>



## CENTAUR™ KS8695PX Register Description

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			111 = 7 x TMULT + 8 cycles
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### 3.3.3 External I/O Access Control Register 2 (EXTACON2 Offset 0x4008)

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:22	-	RW	EB2NPTR External I/O Bank 2 Last Address Pointer This value is the current bank end address. The last address is calculated as {EB2NPTR, 0xffff}.
21:12	-	RW	EB2BPTR External I/O Bank 2 Base Pointer This value is the start address of the External I/O Bank 2. The start address is calculated as EB2BPTR << 16.
11:9	-	RW	EB2TACT External I/O Bank 2 Write Enable/Output Enable Active Time The access time for Bank 2 is defined in units of system clocks. TMULT = 0 000 = 1 cycle 001 = TMULT + 2 cycles 010 = 2 x TMULT + 3 cycles 011 = 3 x TMULT + 4 cycles 100 = 4 x TMULT + 5 cycles 101 = 5 x TMULT + 6 cycles 110 = 6 x TMULT + 7 cycles 111 = 7 x TMULT + 8 cycles  TMULT > 0 000 = 2 <sup>TMULT</sup> + 3 cycles 001 = 1 x 2 <sup>TMULT</sup> + 2 <sup>TMULT</sup> + 3 cycles 010 = 2 x 2 <sup>TMULT</sup> + 2 <sup>TMULT</sup> + 3 cycles 011 = 3 x 2 <sup>TMULT</sup> + 2 <sup>TMULT</sup> + 3 cycles 100 = 4 x 2 <sup>TMULT</sup> + 2 <sup>TMULT</sup> + 3 cycles 101 = 5 x 2 <sup>TMULT</sup> + 2 <sup>TMULT</sup> + 3 cycles 110 = 6 x 2 <sup>TMULT</sup> + 2 <sup>TMULT</sup> + 3 cycles 111 = 7 x 2 <sup>TMULT</sup> + 2 <sup>TMULT</sup> + 3 cycles
8:6	-	RW	EB2TCOH External I/O Bank 2 Chip Select Hold Time The Chip Select Hold time for Bank 2 is defined in units of system clocks. 000 = 1 cycle 001 = TMULT + 2 cycles 010 = 2 x TMULT + 3 cycles 011 = 3 x TMULT + 4 cycles 100 = 4 x TMULT + 5 cycles 101 = 5 x TMULT + 6 cycles 110 = 6 x TMULT + 7 cycles 111 = 7 x TMULT + 8 cycles
5:3	-	RW	EB2TACS External I/O Bank 2 Address Setup Time before ECSN



## CENTAUR™ KS8695PX Register Description

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			<p>The address setup time for Bank 2 is defined in units of system clocks.</p> <p>000 = 0 cycle</p> <p>001 = TMULT + 1 cycles</p> <p>010 = 2 x TMULT + 2 cycles</p> <p>011 = 3 x TMULT + 3 cycles</p> <p>100 = 4 x TMULT + 4 cycles</p> <p>101 = 5 x TMULT + 5 cycles</p> <p>110 = 6 x TMULT + 6 cycles</p> <p>111 = 7 x TMULT + 7 cycles</p>
2:0	-	RW	<p>EB2TCOS External I/O Bank 2 Chip Select Setup Time before OEN</p> <p>The chip select setup time for Bank 2 is defined in units of system clocks.</p> <p>000 = 1 cycle</p> <p>001 = TMULT + 2 cycles</p> <p>010 = 2 x TMULT + 3 cycles</p> <p>011 = 3 x TMULT + 4 cycles</p> <p>100 = 4 x TMULT + 5 cycles</p> <p>101 = 5 x TMULT + 6 cycles</p> <p>110 = 6 x TMULT + 7 cycles</p> <p>111 = 7 x TMULT + 8 cycles</p>

### 3.3.4 ROM/SRAM/FLASH Control Register 0(ROMCON0 Offset 0x4010)

The KS8695PX has two control registers for ROM, SRAM, and FLASH memory. These registers correspond to the two ROM/SRAM/FLASH banks that are supported by the KS8695PX.

For ROM/SRAM/FLASH bank 0, the external data bus width is determined by the B0SIZE[1:0] pins.

- When B0SIZE[1:0] = "01", the external bus width for ROM/SRAM/FLASH bank 0 is 8 bits.
- When B0SIZE[1:0] = "10", the external bus width for ROM/SRAM/FLASH bank 0 is 16 bits.
- When B0SIZE[1:0] = "11", the external bus width for ROM/SRAM/FLASH bank 0 is 32 bits.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:22	1FFH	RW	<p>RB0NPTR ROM/SRAM/FLASH Bank 0 Next Pointer</p> <p>This value is the current bank end address. The last address is calculated as {RB0NPTR, 0xffff}.</p>
21:12	0	RW	<p>RB0BPTR ROM/SRAM/FLASH Bank 0 Base Pointer</p> <p>This value is the start address of the ROM/SRAM/FLASH Bank 0. The start address is calculated as RB0BPTR &lt;&lt; 16.</p>
11:7	0	RO	Reserved



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6:4	111B	RW	<p>RB0TACC ROM/SRAM/FLASH Bank 0 Access Cycle Time</p> <p>The access cycle time is defined in unit of system clock. Note that the write cycle access time is at least 3 cycles.</p> <p>000 = 3 cycles if TMULT = 0 for write cycles</p> <p>000 = TMULT + 2 cycles if TMULT &gt; 0 for write cycles</p> <p>000 = TMULT + 2 cycles for read cycles</p> <p>001 = 2 x TMULT + 3 cycles</p> <p>010 = 3 x TMULT + 4 cycles</p> <p>011 = 4 x TMULT + 5 cycles</p> <p>100 = 5 x TMULT + 6 cycles</p> <p>101 = 6 x TMULT + 7 cycles</p> <p>110 = 7 x TMULT + 8 cycles</p> <p>111 = 8 x TMULT + 9 cycles</p>
3:2	11B	RW	<p>RB0TPA ROM/SRAM/FLASH Bank 0 Page Address Access Time</p> <p>The access cycle time is specified in unit of system clock.</p> <p>00 = TMULT + 2 cycles</p> <p>01 = 2 x TMULT + 3 cycles</p> <p>10 = 3 x TMULT + 4 cycles</p> <p>11 = 4 x TMULT + 5 cycles</p>
1:0	0	RW	<p>RB0PMC ROM/SRAM/FLASH Bank 0 Page Mode Configuration</p> <p>The RB0PMC configures the access size in page mode.</p> <p>00 = Normal ROM</p> <p>01 = 4-word page</p> <p>10 = 8 word page</p> <p>11 = 16 word page</p>

### 3.3.5 ROM/SRAM/FLASH Control Register 1 (ROMCON1 Offset 0x4014)

The KS8695PX has two control registers for ROM, SRAM, and FLASH memory. These registers correspond to the two ROM/SRAM/FLASH banks that are supported by the KS8695PX. The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:22	-	RW	<p>RB1NPTR ROM/SRAM/FLASH Bank 1 Next Pointer</p> <p>This value is the current bank end address. The last address is calculated as {RB1NPTR, 0xffff}.</p>
21:12	-	RW	<p>RB1BPTR ROM/SRAM/FLASH Bank 1 Base Pointer</p> <p>This value is the start address of the ROM/SRAM/FLASH Bank 1. The start address is calculated as RB1BPTR &lt;&lt; 16.</p>
11:7	0	RO	Reserved
6:4	-	RW	<p>RB1TACC ROM/SRAM/FLASH Bank 1 Access Cycle Time</p> <p>The access cycle time is defined in unit of system clock. Note that the write cycle access time is at least 3 cycles.</p> <p>000 = 3 cycles if TMULT = 0 for write cycles</p> <p>000 = TMULT + 2 cycles if TMULT &gt; 0 for write cycles</p>





## CENTAUR™ KS8695PX Register Description

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			000 = TMULT + 2 cycles for read cycles 001 = 2 x TMULT + 3 cycles 010 = 3 x TMULT + 4 cycles 011 = 4 x TMULT + 5 cycles 100 = 5 x TMULT + 6 cycles 101 = 6 x TMULT + 7 cycles 110 = 7 x TMULT + 8 cycles 111 = 8 x TMULT + 9 cycles
3:2	-	RW	RB1TPA ROM/SRAM/FLASH Bank 1 Page Address Access Time The access cycle time is specified in unit of system clock. 00 = TMULT + 2 cycles 01 = 2 x TMULT + 3 cycles 10 = 3 x TMULT + 4 cycles 11 = 4 x TMULT + 5 cycles
1:0	-	RW	RB1PMC ROM/SRAM/FLASH Bank 1 Page Mode Configuration The RB1PMC configures the access size in page mode. 00 = Normal ROM 01 = 4-word page 10 = 8 word page 11 = 16 word page

### 3.3.6 External I/O and ROM/SRAM/FLASH General Register (ERGCON Offset 0x4020)

The KS8695PX supports 8/16/32-bit external ROM/SRAM/FLASH memory and I/O interfaces. By programming this register, the data width of the ROM/SRAM/FLASH memory and I/O interfaces can be controlled.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:30	0	RO	Reserved
29:28	3H	RW	TMULT External I/O and ROM/SRAM/FLASH Time Multiplier 00 = Multiply by 0 01 = Multiply by 1 10 = Multiply by 2 11 = Multiply by 3
27:24	0	RO	Reserved
23:22	0	RW	Reserved
21:20	0	RW	DSX2 Data Width for External I/O Bank 2 00 = disabled 01 = Byte ( 8 bits ) 10 = Half-word (16 bits) 11 = Word (32 bits)
19:18	0	RW	DSX1 Data Width for External I/O Bank 1 00 = disabled



## CENTAUR™ KS8695PX Register Description

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			01 = Byte ( 8 bits ) 10 = Half-word (16 bits) 11 = Word (32 bits)
17:16	0	RW	DSX0 Data Width for External I/O Bank 0 00 = disabled 01 = Byte ( 8 bits ) 10 = Half-word (16 bits) 11 = Word (32 bits)
15:8	0	RO	Reserved
7:6	0	RW	Reserved
5:4	0	RW	Reserved
3:2	0	RW	DSR1 Data Width for ROM/SRAM/FLASH Bank 1 00 = disabled 01 = Byte ( 8 bits ) 10 = Half-word (16 bits) 11 = Word (32 bits)
1:0	-	RW	DSR0 Data Width for ROM/SRAM/FLASH Bank 0 00 = disabled 01 = Byte ( 8 bits ) 10 = Half-word (16 bits) 11 = Word (32 bits)  Note: DSR0's value is derived from B0SIZE[1:0] upon power on reset. After power on reset, it can be written with 00B to disable the bank or the value of B0SIZE[1:0] to enable the bank. Any other written values are ignored.

### 3.3.7 SDRAM Control Register 0(SDCON0 Offset 0x4030)

The KS8695PX has two control registers for SDRAM memory. These registers correspond to the two SDRAM banks that are supported by the KS8695PX.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:22	-	RW	DB0NPTR SDRAM Bank 0 Last Address Pointer This value is the current bank end address. The last address is calculated as {DB0NPTR, 0xffff}.
21:12	-	RW	DB0BPTR SDRAM Bank 0 Base Pointer This value is the start address of the SDRAM Bank 0. The start address is calculated as DB0BPTR << 16.
11:10	00	RO	Reserved
9:8	-	RW	DB0CAB SDRAM Bank 0 Column Address Bits This field selects the number of column address bits for the SDRAM. 00 = 8 bits 01 = 9 bits 10 = 10 bits



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			11 = 11 bits
7:4	0x0	RO	Reserved
3	-	RW	DB0BNUM SDRAM Bank 0 Number of Banks 0 = 2 Bank Device 1 = 4 Bank Device
2:1	00	RW	DB0DBW SDRAM Bank 0 Data Bus Width 00 = Disabled 01 = 8 Bit 10 = 16 Bits 11 = 32 Bits
0	0	RO	Reserved

### 3.3.8 SDRAM Control Register 1(SDCON1 Offset 0x4034)

The KS8695PX has two control registers for SDRAM memory. These registers correspond to the two SDRAM banks that are supported by the KS8695PX.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:22	-	RW	DB1NPTR SDRAM Bank 1 Last Address Pointer This value is the current bank end address. The last address is calculated as {DB1NPTR, 0xffff}.
21:12	-	RW	DB1BPTR SDRAM Bank 1 Base Pointer This value is the start address of the SDRAM Bank 1. The start address is calculated as DB1BPTR << 16.
11:10	0x000	RO	Reserved
9:8	-	RW	DB1CAB SDRAM Bank 1 Column Address Bits This field selects the number of column address bits for the SDRAM. 00 = 8 bits 01 = 9 bits 10 = 10 bits 11 = 11 bits
7:4	0x0	RO	Reserved
3	-	RW	DB1BNUM SDRAM Bank 1 Number of Banks 0 = 2 Bank Device 1 = 4 Bank Device
2:1	00	RW	DB1DBW SDRAM Bank 1 Data Bus Width 00 = Disabled 01 = 8 Bit 10 = 16 Bits 11 = 32 Bits
0	0	RO	Reserved



## CENTAUR™ KS8695PX Register Description

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### 3.3.9 SDRAM General Control Register (SDGCON Offset 0x4038)

This register controls the global settings of the SDRAM controller.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:9	0x0	RO	Reserved
8	0	RW	Reserved
7:4	0x0	RO	Reserved
3:2	-	RW	SDTRC SDRAM RAS to CAS Latency 00 = 1 Cycle 01 = 2 Cycles 10 = 3 Cycles 11 = 4 Cycles
1:0	-	RW	SDCAS SDRAM CAS Latency 00 = 1 Cycle 01 = 2 Cycles 10 = 3 Cycles 11 = 4 Cycles

### 3.3.10 SDRAM Buffer Control Register (SDBCON Offset 0x403C)

This register configures the function of the read and write buffer in the memory controller.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0	RO	SDESTA SDRAM Engine Status Bit 0 = SDRAM engine is idle. 1 = SDRAM engine is busy.
30:24	0x00	RO	Reserved
24	0	RW	RBUFBDIS Read Buffer Burst Enable. This bit controls the read burst length for on-chip AMBA bus incremental burst when RBUFEN is reset. This bit is ignored when RBUFEN is set. 0 – Read buffer burst is disabled for the incremental burst. 1 – Read buffer burst is enabled for the incremental burst.
23	0	RW	WFIFOEN Write FIFO Enable. 0 – Write FIFO is disabled. 1 – Write FIFO is enabled.
22	0	RW	RBUFEN Read Buffer Enable. 0 – Read buffer is disabled. 1 – Read buffer is enabled.
21	0	RW	FLUSHWFIFO Flush Write FIFO Writing a “1” to this bit causes the write FIFO to be flushed to the SDRAM memory. After the flush, this bit is cleared.
20	0	RW	RBUFINV Read Buffer Invalidate



## CENTAUR™ KS8695PX Register Description

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			Writing a "1" to this bit invalidates the read buffer. After the invalidation, this bit is cleared.
19:18	0	RO	Reserved
17:16	00	RW	SDINI SDRAM Initialization Control After the command is issued, SDINI is reset. 00 = Normal Operation. 01 = Issue a Precharge All Banks Command to the SDRAM. 10 = Issue a Mode Command to the SDRAM. 11 = Issue a NOP to the SDRAM.
15:14	00	RO	Reserved
13:0	-	RW	SDMODE SDRAM Mode Register Program Value During the issue of mode command to the SDRAM, SDMODE[13:0] also goes out to ADDR[13:0].

#### 3.3.11 SDRAM Refresh Timer Register (REFTIM Offset 0x4040)

The refresh timer register is a 16-bit read/write register that is programmed with the number of network clocks (XCLK1) ticks that should be counted between SDRAM refresh cycles. For example, for the common refresh period of 16 $\mu$ s, and a network clock frequency of 25MHz, the following value should be programmed into it:  
 $16 \times 10^{-6} \times 25 \times 10^6 = 400$

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:16	0x0	RO	Reserved
15:0	0x0	RW	REFTIM Refresh Timer Value A value of 0 disables refresh timer.

## 3.4 WAN DMA Registers

#### 3.4.1 WAN MAC DMA Transmit Control Register (WMDTXC Offset 0x6000)

The WAN MAC DMA transmit control register establishes the transmit operating modes and commands for the WAN port. This register should be one of the last SCRs to be written as part of the transmit initialization.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0	WO	WMTRST WAN DMA Soft Reset When set, the WAN MAC DMA block is reset. All registers in the WAN MAC DMA block will be reset to the default values.
30		RO	Reserved
29:24	0x00	RW	WMTBS WAN DMA Transmit Burst Size



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			This field indicates the maximum number of words to be transferred in one DMA transaction. If reset, the WAN MAC DMA burst size is limited only by the amount of data stored in the transmit buffer before issuing a bus request. The WMTBS can be programmed with permissible values 0, 1, 2, 4, 8, 16, or 32. After reset, the WMTBS default is 0, i.e. unlimited.
23:19	0x00	RO	Reserved
18	0	RW	WMTUCG WAN MAC Transmit UDP Checksum Generate When set, the KS8695PX will generate correct UDP checksum for outgoing UDP/IP frames at WAN port. When this bit is set, ADD CRC should also turn on.
17	0	RW	WMTTCG WAN MAC Transmit TCP Checksum Generate When set, the KS8695PX will generate correct TCP checksum for outgoing TCP/IP frames at WAN port. When this bit is set, ADD CRC should also turn on.
16	0	RW	WMTICG WAN MAC Transmit IP Checksum Generate When set, the KS8695PX will generate correct IP checksum for outgoing IP frames at WAN port. When this bit is set, ADD CRC should also turn on.
15:10	0x00	RO	Reserved
9	0	RW	WMTFCE WAN MAC Transmit Flow Control Enable When this bit is set and the KS8695PX is in Full Duplex mode, flow control is enabled and the KS8695PX will transmit a PAUSE frame when the MAC DMA Receive Buffer capacity has reached a level that may cause the buffer to overflow. When this bit is set and the KS8695PX is in Half Duplex mode, back-pressure flow control is enabled. When this bit is cleared, no transmit flow control is enabled.
8	0	RW	WMTLB WAN MAC DMA Loop Back Mode Select the KS8695PX WAN port in loopback operation modes. When set, the packet to be sent will be returned at the MAC interface.
7:3	0x0	RO	Reserved
2	0	RW	WMTEP WAN MAC DMA Transmit Enable Padding When set, the KS8695PX automatically adds a padding field to a packet shorter than 64 bytes. Note: Setting this bit automatically enables Add CRC feature.
1	0	RW	WMTAC WAN MAC DMA Transmit Add CRC When set, the KS8695PX appends the CRC to the end of the transmission frame.
0	0	RW	WMTE WAN MAC DMA TX Enable When the bit is set, the MDMA TX block is enabled and placed in a running state. When reset, the transmission process is placed in the stopped state after completing the transmission of the current frame. The stop transmission command is effective only when the transmission process is in the running state.

#### 3.4.2 WAN MAC DMA Receive Control Register (WMDRXC Offset 0x6004)



## CENTAUR™ KS8695PX Register Description

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The WAN MAC DMA receive control register establishes the receive operating modes and commands for the WAN port. This register should be one of the last SCRs to be written as part of the receive initialization.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:30	00	RO	Reserved
29:24	0x00	RW	WMRBS WAN MAC Receive Burst Size This field indicates the maximum number of words to be transferred in one DMA transaction. If reset, the WAN MAC DMA burst size is limited only by the amount of data stored in the receive buffer before issuing a bus request. The WMRBS can be programmed with permissible values 0, 1, 2, 4, 8, 16, or 32. After reset, the WMRBS default is 0, i.e. unlimited.
23:19	0x00	RO	Reserved
18	0	RW	WMRUCC WAN MAC Receive UDP Checksum Check When set, the KS8695PX will check for correct UDP checksum for incoming UDP/IP frames at WAN port. Packets received with incorrect UDP checksum will be discarded.
17	0	RW	WMRTCG WAN MAC Receive TCP Checksum Check When set, the KS8695PX will check for correct TCP checksum for incoming TCP/IP frames at WAN port. Packets received with incorrect TCP checksum will be discarded.
16	0	RW	WMRICG WAN MAC Receive IP Checksum Check When set, the KS8695PX will check for correct IP checksum for incoming IP frames at WAN port. Packets received with incorrect IP checksum will be discarded.
15:10	0x00	RO	Reserved
9	0	RW	WMRFCE WAN MAC Receive Flow Control Enable When this bit is set and the KS8695PX is in Full Duplex mode, flow control is enabled and the KS8695PX will acknowledge a PAUSE frame from the WAN port, i.e. the outgoing packets will be pending in the transmit buffer until the PAUSE control timer expires. This field has no meaning in half-duplex mode and should be programmed to 0. When this bit is cleared, no flow control is enabled.
8:7	00	RO	Reserved
6	0	RW	WMRB WAN MAC Receive Broadcast When set, the WAN MAC receive all broadcast frames.
5	0	RW	WMRM WAN MAC Receive Multicast When set, the WAN MAC receive all multicast frames (including broadcast).
4	0	RW	WMRU WAN MAC Receive Unicast When set, the WAN MAC receive unicast frames that match the 48-bit Station Address of the WAN MAC.
3	0	RW	WMRE WAN MAC DMA Receive Error Frame When set, the KS8695PX will pass the errors frames received to the host.





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			Error frames include runt frames, oversized frames, CRC errors.
2	0	RW	WMRA WAN MAC DMA Receive All When set, the KS8695PX receives all incoming frames, regardless of its destination address.
1	0	RO	Reserved
0	0	RW	WMRE WAN MAC DMA RX Enable When the bit is set, the DMA RX block is enabled and placed in a running state. When reset, the receive process is placed in the stopped state after completing the reception of the current frame. The stop transmission command is effective only when the reception process is in the running state.

### 3.4.3 WAN MAC DMA Transmit Start Command Register (WMDTSC Offset 0x6008)

This register is written by the CPU when packets in the WAN data buffer need to be transmitted. The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	0x0	WO	WTSC WAN Transmit Start Command When written with any value, the WAN Transmit DMA checks for frames to be transmitted. If no descriptor is available, the transmit process returns to suspended state. If descriptors are available, the transmit process starts or resumes. This bit is self-clearing.

### 3.4.4 WAN MAC DMA Receive Start Command Register (WMDRSC Offset 0x600C)

This register is written by the CPU when there are frame data in receive buffer to be processed.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	0x0	WO	WRSC WAN Receive Start Command When written with any value, the WAN Receive DMA checks for descriptors to be acquired. If no descriptor is available, the receive process returns to suspended state and wait for the next receive restart command. If descriptors are available, the receive process resumes. This bit is self-clearing.

### 3.4.5 WAN Transmit Descriptor List Base Address Register (WTDLB Offset 0x6010)

This register is used for WAN Transmit descriptor list base address register. The register is used to point to the start of the appropriate descriptor list. Writing to this register is permitted only when its respective process is in the stopped state. When stopped, the register must be written before the respective **START** command is given.

Note: The descriptor lists must be Word (32-bit) aligned. The KS8695PX behavior is unpredictable when the lists are not word-aligned.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
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## CENTAUR™ KS8695PX Register Description

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31:2	0x0	RW	WSTL WAN Start of Transmit List Note: Write can only occur when the transmit process stopped.
1:0	00	RO	Reserved

### 3.4.6 WAN Receive Descriptor List Base Address Register (WRDLB Offset 0x6014)

This register is used for WAN Receive descriptor list base address register. The register is used to point to the start of the appropriate descriptor list. Writing to this register is permitted only when its respective process is in the stopped state. When stopped, the register must be written before the respective **START** command is given.

Note: The descriptor lists must be Word (32-bit) aligned. The KS8695PX behavior is unpredictable when the lists are not word-aligned.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:2	0x0	RW	WSRL WAN Start of Receive List Note: Write can only occur when the transmit process stopped.
1:0	00	RO	Reserved

### 3.4.7 WAN MAC Station Address Low Register (WMAL Offset 0x6018)

Station Address is used to define the individual destination address the KS8695PX WAN port will respond to when receiving frames. Network addresses are generally expressed in the form of 01:23:45:67:89:AB, where the bytes are received left to right, and the bits within each byte are received right to left (LSB to MSB). The actual transmitted and received bits are in the order of 10000000 11000100 10100010 11100110 10010001 11010101.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	0x0	RW	WMAL WAN MAC Station Address Low 4 bytes The least significant word of the WAN MAC station address.

### 3.4.8 WAN MAC Station Address High Register (WMAH Offset 0x601C)

Station Address is used to define the individual destination address the KS8695PX WAN port will respond to when receiving frames. Network addresses are generally expressed in the form of 01:23:45:67:89:AB, where the bytes are received left to right, and the bits within each byte are received right to left (LSB to MSB). The actual transmitted and received bits are in the order of 10000000 11000100 10100010 11100110 10010001 11010101.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:16	0x0	RO	Reserved
15:0	0x0	RW	WMAH WAN MAC Station Address High 2 bytes The most significant word of the WAN MAC station address.

### 3.4.9 WAN MAC Additional Station Address Low Register (WMAAL0-15)



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The KS8695PX supports 16 additional MAC addresses for MAC address filtering. This MAC address is used to define one of the 16 destination addresses that the KS8695PX will respond to when receiving frames on the WAN port. Network addresses are generally expressed in the form of 01:23:45:67:89:AB, where the bytes are received left to right, and the bits within each byte are received right to left (LSB to MSB). The actual transmitted and received bits are in the order of 10000000 11000100 10100010 11100110 10010001 11010101.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	--	RW	WMAAL0 WAN MAC Additional Station Address 0 Low 4 bytes The least significant word of the additional WAN MAC 0 station address.

#### 3.4.10 WAN MAC Additional Station Address High Register (WMAAH0-15)

The KS8695PX supports 16 additional MAC addresses for MAC address filtering. This MAC address is used to define one of the 16 destination addresses that the KS8695PX will respond to when receiving frames on the WAN port. Network addresses are generally expressed in the form of 01:23:45:67:89:AB, where the bytes are received left to right, and the bits within each byte are received right to left (LSB to MSB). The actual transmitted and received bits are in the order of 10000000 11000100 10100010 11100110 10010001 11010101.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0	RW	WMAA0E WAN MAC Additional Station Address 0 Enable When set, the additional WAN MAC address is enabled for received frames. When reset, the additional WAN MAC address is disabled.
30:16	0x0	RO	Reserved
15:0	--	RW	WMAAH0 WAN MAC Additional Station Address 0 High 2 bytes The most significant word of the additional WAN MAC 0 station address.

The following table shows the register map for all 16 additional WAN MAC address registers.

REGISTER	IDENTIFIER	OFFSET
ADD MAC Low 0	WMAAL0	0x6080
ADD MAC High 0	WMAAH0	0x6084
ADD MAC Low 1	WMAAL1	0x6088
ADD MAC High 1	WMAAH1	0x608C
ADD MAC Low 2	WMAAL2	0x6090
ADD MAC High 2	WMAAH2	0x6094
ADD MAC Low 3	WMAAL3	0x6098
ADD MAC High 3	WMAAH3	0x609C
ADD MAC Low 4	WMAAL4	0x60A0
ADD MAC High 4	WMAAH4	0x60A4
ADD MAC Low 5	WMAAL5	0x60A8
ADD MAC High 5	WMAAH5	0x60AC
ADD MAC Low 6	WMAAL6	0x60B0



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ADD MAC High 6	WMAAH6	0x60B4
ADD MAC Low 7	WMAAL7	0x60B8
ADD MAC High 7	WMAAH7	0x60BC
ADD MAC Low 8	WMAAL8	0x60C0
ADD MAC High 8	WMAAH8	0x60C4
ADD MAC Low 9	WMAAL9	0x60C8
ADD MAC High 9	WMAAH9	0x60CC
ADD MAC Low 10	WMAAL10	0x60D0
ADD MAC High 10	WMAAH10	0x60D4
ADD MAC Low 11	WMAAL11	0x60D8
ADD MAC High 11	WMAAH11	0x60DC
ADD MAC Low 12	WMAAL12	0x60E0
ADD MAC High 12	WMAAH12	0x60E4
ADD MAC Low 13	WMAAL13	0x60E8
ADD MAC High 13	WMAAH13	0x60EC
ADD MAC Low 14	WMAAL14	0x60F0
ADD MAC High 14	WMAAH14	0x60F4
ADD MAC Low 15	WMAAL15	0x60F8
ADD MAC High 15	WMAAH15	0x60FC

### 3.5 LAN DMA Registers

#### 3.5.1 LAN MAC DMA Transmit Control Register (LMDTXC Offset 0x8000)

The LAN MAC DMA transmit control register establishes the transmit operating modes and commands for the LAN port. This register should be one of the last SCRs to be written as part of the transmit initialization.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0	WO	LMTRST LAN DMA Soft Reset When set, the LAN MAC DMA block is reset. All registers in the LAN MAC DMA block will be reset to the default values.
30	0	RO	Reserved
29:24	0x00	RW	LMTBS LAN DMA Transmit Burst Size This field indicates the maximum number of words to be transferred in one DMA transaction. If reset, the LAN MAC DMA burst size is limited only by the amount of data stored in the transmit buffer before issuing a bus request. The LMTBS can be programmed with permissible values 0, 1, 2, 4, 8, 16, or 32. After reset, the LMTBS default is 0, i.e. unlimited.
23:19	0x00	RO	Reserved
18	0	RW	LMTUCG LAN MAC Transmit UDP Checksum Generate When set, the KS8695PX will generate correct UDP checksum for



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			outgoing UDP/IP frames at LAN port. When this bit is set, ADD CRC should also turn on.
17	0	RW	LMTTCG LAN MAC Transmit TCP Checksum Generate When set, the KS8695PX will generate correct TCP checksum for outgoing TCP/IP frames at LAN port. When this bit is set, ADD CRC should also turn on.
16	0	RW	LMTICG LAN MAC Transmit IP Checksum Generate When set, the KS8695PX will generate correct IP checksum for outgoing IP frames at LAN port. When this bit is set, ADD CRC should also turn on.
15:10	0x00	RO	Reserved
9	0	RW	LMTFCE LAN MAC Transmit Flow Control Enable When this bit is set and the KS8695PX is in Full Duplex mode, flow control is enabled and the KS8695PX will transmit a PAUSE frame when the MAC DMA Receive Buffer capacity has reached a level that may cause the buffer to overflow. When this bit is set and the KS8695PX is in Half Duplex mode, back-pressure flow control is enabled. When this bit is cleared, no transmit flow control is enabled.
8	0	RW	LMTLB LAN MAC DMA Loop Back Mode Select the KS8695PX LAN port in loopback operation modes. When set, the packet to be sent will be returned at the MAC interface.
7:3	0x0	RO	Reserved
2	0	RW	LMTEP LAN MAC DMA Transmit Enable Padding When set, the KS8695PX automatically adds a padding field to a packet shorter than 64 bytes. Note: Setting this bit automatically enables Add CRC feature.
1	0	RW	LMTAC LAN MAC DMA Transmit Add CRC When set, the KS8695PX appends the CRC to the end of the transmission frame.
0	0	RW	LMTE LAN MAC DMA TX Enable When the bit is set, the DMA TX block is enabled and placed in a running state. When reset, the transmission process is placed in the stopped state after completing the transmission of the current frame. The stop transmission command is effective only when the transmission process is in the running state.

### 3.5.2 LAN MAC DMA Receive Control Register (LMDRXC Offset 0x8004)

The LAN MAC DMA receive control register establishes the receive operating modes and commands for the LAN port. This register should be one of the last SCRs to be written as part of the receive initialization.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:30	00	RO	Reserved



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29:24	0x00	RW	<p>LMRBS LAN DMA Receive Burst Size</p> <p>This field indicates the maximum number of words to be transferred in one DMA transaction. If reset, the LAN MAC DMA burst size is limited only by the amount of data stored in the receive buffer before issuing a bus request. The LMRBS can be programmed with permissible values 0,1, 2, 4, 8, 16, or 32.</p> <p>After reset, the LMRBS default is 0, i.e. unlimited.</p>
23:19	0x00	RO	Reserved
18	0	RW	<p>LMRUCC LAN MAC Receive UDP Checksum Check</p> <p>When set, the KS8695PX will check for correct UDP checksum for incoming UDP/IP frames at LAN port. Packets received with incorrect UDP checksum will be discarded.</p>
17	0	RW	<p>LMRTCG LAN MAC Receive TCP Checksum Check</p> <p>When set, the KS8695PX will check for correct TCP checksum for incoming TCP/IP frames at LAN port. Packets received with incorrect TCP checksum will be discarded.</p>
16	0	RW	<p>LMRICG LAN MAC Receive IP Checksum Check</p> <p>When set, the KS8695PX will check for correct IP checksum for incoming IP frames at LAN port. Packets received with incorrect IP checksum will be discarded.</p>
15:10	0x00	RO	Reserved
9	0	RW	<p>LMRFCE LAN MAC Receive Flow Control Enable</p> <p>When this bit is set and the KS8695PX is in Full Duplex mode, flow control is enabled and the KS8695PX will acknowledge a PAUSE frame from the LAN port, i.e. the outgoing packets will be pending in the transmit buffer until the PAUSE control timer expires. This field has no meaning in half-duplex mode and should be programmed to 0.</p> <p>When this bit is cleared, no flow control is enabled.</p>
8:7	00	RO	Reserved
6	0	RW	<p>LMRB LAN MAC Receive Broadcast</p> <p>When set, the LAN MAC receive all broadcast frames.</p>
5	0	RW	<p>LMRM LAN MAC Receive Multicast</p> <p>When set, the LAN MAC receive all multicast frames (including broadcast).</p>
4	0	RW	<p>LMRU LAN MAC Receive Unicast</p> <p>When set, the LAN MAC receive unicast frames that match the 48-bit Station Address of the LAN MAC.</p>
3	0	RW	<p>LMRE LAN MAC DMA Receive Error Frame</p> <p>When set, the KS8695PX will pass the errors frames received to the host.</p> <p>Error frames include runt frames, oversized frames, CRC errors.</p>
2	0	RW	<p>LMRA LAN MAC DMA Receive All</p> <p>When set, the KS8695PX receives all incoming frames, regardless of its destination address.</p>
1	0	RO	Reserved
0	0	RW	<p>LMRE LAN MAC DMA RX Enable</p> <p>When the bit is set, the DMA RX block is enabled and placed in a</p>



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			running state. When reset, the receive process is placed in the stopped state after completing the reception of the current frame. The stop transmission command is effective only when the reception process is in the running state.
--	--	--	--

#### 3.5.3 LAN MAC DMA Transmit Start Command Register (LMDTSC Offset 0x8008)

This register is written by the the CPU when packets in the LAN data buffer need to be transmitted.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	0x0	WO	LTSC LAN Transmit Start Command When written with any value, the LAN Transmit DMA checks for frames to be transmitted. If no descriptor is available, the transmit process returns to suspended state. If descriptors are available, the transmit process starts or resumes. This bit is self-clearing.

#### 3.5.4 LAN MAC DMA Receive Start Command Register (LMDRSC Offset 0x800C)

This register is written by the the CPU when there are frame data in receive buffer to be processed.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	0x0	WO	LRSC LAN Receive Start Command When written with any value, the WLAN Receive DMA checks for descriptors to be acquired. If no descriptor is available, the receive process returns to suspended state and wait for the next receive restart command. If descriptors are available, the receive process resumes. This bit is self-clearing.

#### 3.5.5 LAN Transmit Descriptor List Base Address Register (LTDLB Offset 0x8010)

This register is used for LAN Transmit descriptor list base address register. The register is used to point to the start of the appropriate descriptor list. Writing to this register is permitted only when its respective process is in the stopped state. When stopped, the register must be written before the respective **START** command is given.

Note: The descriptor lists must be Word (32-bit) aligned. The KS8695PX behavior is unpredictable when the lists are not word-aligned.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:2	0x0	RW	LSTL LAN Start of Transmit List Note: Write can only occur when the transmit process stopped.
1:0	00	RO	Reserved





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### 3.5.6 LAN Receive Descriptor List Base Address Register (LRDLB Offset 0x8014)

This register is used for LAN Receive descriptor list base address register. The register is used to point to the start of the appropriate descriptor list. Writing to this register is permitted only when its respective process is in the stopped state. When stopped, the register must be written before the respective **START** command is given.

Note: The descriptor lists must be Word (32-bit) aligned. The KS8695PX behavior is unpredictable when the lists are not word-aligned.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:2	0x0	RW	LSRL LAN Start of Receive List Note: Write can only occur when the transmit process stopped.
1:0	00	RO	Reserved

### 3.5.7 LAN MAC Station Address Low Register (LMAL Offset 0x8018)

Station Address is used to define the individual destination address the KS8695PX LAN port will respond to when receiving frames. Network addresses are generally expressed in the form of 01:23:45:67:89:AB, where the bytes are received left to right, and the bits within each byte are received right to left (LSB to MSB). The actual transmitted and received bits are in the order of 10000000 11000100 10100010 11100110 10010001 11010101.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	0x0	RW	LMAL LAN MAC Station Address Low 4 bytes The least significant word of the LAN MAC station address.

### 3.5.8 LAN MAC Station Address High Register (LMAH Offset 0x801C)

Station Address is used to define the individual destination address the KS8695PX LAN port will respond to when receiving frames. Network addresses are generally expressed in the form of 01:23:45:67:89:AB, where the bytes are received left to right, and the bits within each byte are received right to left (LSB to MSB). The actual transmitted and received bits are in the order of 10000000 11000100 10100010 11100110 10010001 11010101.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:16	0x0	RO	Reserved
15:0	0x0	RW	LMAL LAN MAC Station Address High 2 bytes The most significant word of the LAN MAC station address.

### 3.5.9 LAN MAC Additional Station Address Low Register (LMAAL0-15)

The KS8695PX supports 16 additional MAC addresses for MAC address filtering. This MAC address is used to define one of the 16 destination addresses that the KS8695PX will respond to when receiving frames on the LAN port. Network addresses are generally expressed in the form of 01:23:45:67:89:AB, where the bytes are received left to right, and the bits within each byte are





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received right to left (LSB to MSB). The actual transmitted and received bits are in the order of 10000000 11000100 10100010 11100110 10010001 11010101.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	--	RW	LMAAL0 LAN MAC Additional Station Address 0 Low 4 bytes The least significant word of the additional LAN MAC 0 station address.

#### 3.5.10 LAN MAC Additional Station Address High Register (LMAAH0-15)

The KS8695PX supports 16 additional MAC addresses for MAC address filtering. This MAC address is used to define one of the 16 destination addresses that the KS8695PX will respond to when receiving frames on the LAN port. Network addresses are generally expressed in the form of 01:23:45:67:89:AB, where the bytes are received left to right, and the bits within each byte are received right to left (LSB to MSB). The actual transmitted and received bits are in the order of 10000000 11000100 10100010 11100110 10010001 11010101.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0	RW	LMAA0E LAN MAC Additional Station Address 0 Enable When set, the additional LAN MAC address is enabled for received frames. When reset, the additional LAN MAC address is disabled.
30:16	0x0	RO	Reserved
15:0	--	RW	LMAAH0 LAN MAC Additional Station Address 0 High 2 bytes The most significant word of the additional LAN MAC 0 station address.

The following table shows the register map for all 16 additional LAN MAC address registers.

REGISTER	IDENTIFIER	OFFSET
ADD MAC Low 0	LMAAL0	0x8080
ADD MAC High 0	LMAAH0	0x8084
ADD MAC Low 1	LMAAL1	0x8088
ADD MAC High 1	LMAAH1	0x808C
ADD MAC Low 2	LMAAL2	0x8090
ADD MAC High 2	LMAAH2	0x8094
ADD MAC Low 3	LMAAL3	0x8098
ADD MAC High 3	LMAAH3	0x809C
ADD MAC Low 4	LMAAL4	0x80A0
ADD MAC High 4	LMAAH4	0x80A4
ADD MAC Low 5	LMAAL5	0x80A8
ADD MAC High 5	LMAAH5	0x80AC
ADD MAC Low 6	LMAAL6	0x80B0
ADD MAC High 6	LMAAH6	0x80B4
ADD MAC Low 7	LMAAL7	0x80B8
ADD MAC High 7	LMAAH7	0x80BC



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ADD MAC Low 8	LMAAL8	0x80C0
ADD MAC High 8	LMAAH8	0x80C4
ADD MAC Low 9	LMAAL9	0x80C8
ADD MAC High 9	LMAAH9	0x80CC
ADD MAC Low 10	LMAAL10	0x80D0
ADD MAC High 10	LMAAH10	0x80D4
ADD MAC Low 11	LMAAL11	0x80D8
ADD MAC High 11	LMAAH11	0x80DC
ADD MAC Low 12	LMAAL12	0x80E0
ADD MAC High 12	LMAAH12	0x80E4
ADD MAC Low 13	LMAAL13	0x80E8
ADD MAC High 13	LMAAH13	0x80EC
ADD MAC Low 14	LMAAL14	0x80F0
ADD MAC High 14	LMAAH14	0x80F4
ADD MAC Low 15	LMAAL15	0x80F8
ADD MAC High 15	LMAAH15	0x80FC

### 3.6 UART Registers

#### 3.6.1 UART Receive Buffer Register (URRB Offset 0xE000)

The UART Receive Buffer register contains an 8-bit data value received over the UART channel. The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:8	0x0	RO	Reserved
7:0	--	RO	URRBD UART Receive Buffer Data This field contains the data received over the single channel UART. When UART finishes receiving data frame, the Receive Data Ready bit in the Line Status Register will be set. Note: whenever the URRBD is read, the Receive Data Ready bit in the Line Status Register is automatically cleared.

#### 3.6.2 UART Transmit Holding Register (URTH Offset 0xE004)

The UART Transmit Holding register contains an 8-bit data value to be transmitted over the UART channel.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:8	0x0	RO	Reserved
7:0	--	WO	URTHD UART Transmit Holding Data



## CENTAUR™ KS8695PX Register Description

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			<p>This field contains the data to be transmitted over the single channel UART. Whenever the URTHD is written, the Transmit Holding Register Empty bit in the Line Status Register is automatically cleared to '0' until the UART finishes transmitting the data.</p> <p>Note: software should ensure that the Transmit Holding Register Empty bit in the Line Status Register is '1' before writing to this register to prevent from over-writing the current transmit data.</p>
--	--	--	---

#### 3.6.3 UART FIFO Control Register (URFC Offset 0xE008)

The UART FIFO Control register provides control over transmitter and receiver FIFOs.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:8	0x0	RO	Reserved
7:6	00	RW	URFRT UART Receive FIFO Trigger Level This field controls the trigger level for the receive FIFO. 00 = 1 Byte 01 = 4 Bytes 10 = 8 Bytes 11 = 14 Bytes
5:3	000	RO	Reserved
2	0	RW	URTFR UART Transmit FIFO Reset When set, the transmit state machine will be reset, and the transmit FIFO will be emptied. Writing '0' has no effect. Note: This bit will be self-cleared to 0 after 1 is written.
1	0	RW	URRFR UART Receive FIFO Reset When set, the receive FIFO state machine will be reset, and receive FIFO will be emptied. Writing '0' has no effect. Note: This bit will be self-cleared to 0 after 1 is written.
0	0	RW	URFE UART FIFO Enable When set, both the transmit and receive FIFOs are enabled. (UART is in 16550 mode) When reset, both the transmit and receive FIFOs are disabled. (UART is in 16450 mode) Note that when UART changes from FIFO to character mode or vice versa, data in the FIFOs are automatically cleared. This bit must be set when other control bits in this register are written to or they will not be programmed.

#### 3.6.4 UART Line Control Register (URLC Offset 0xE00C)

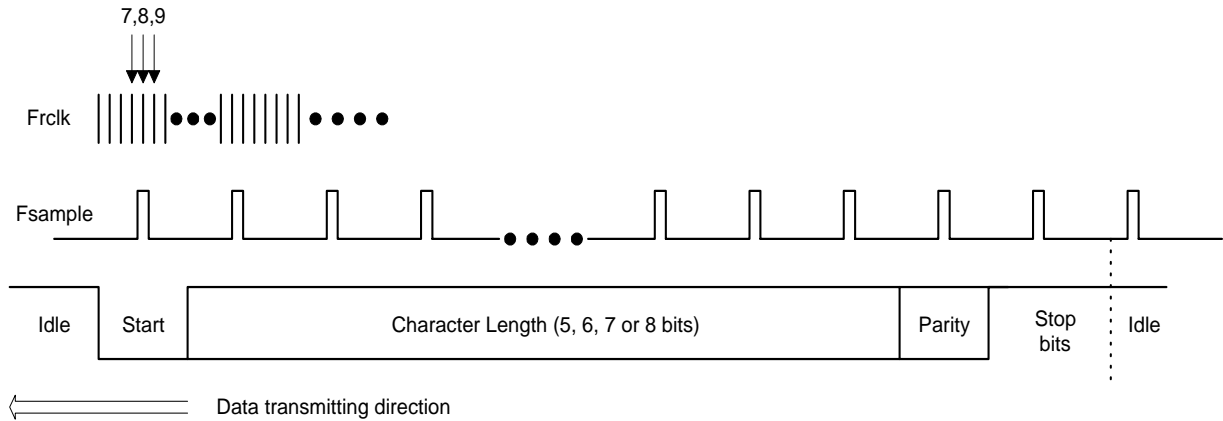
The UART Line Control register basically specifies the asynchronous data frame for transmitting and receiving as seen below.

Figure 8 UART Line Control



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When the bus(one bit serial bus) is idle, it stays at high. The first high-to-low transition is detected as the Start bit. Start bit is Low and Stop bit is High. Due to the noise, a short glitch might happen on the bus. To avoid detecting the wrong Start bit, three samples at clock (Frclk) 7, 8, and 9 after high-to-low transition are taken on the bus. If at least two out of three samples are Low, then Start bit is detected; otherwise, the high-to-low transition is treated as a glitch. Frclk and Fsample will be defined at Baud Rate Divisor Register section.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:7	0x0	RO	Reserved
6	0	RW	URSBC UART Set Break Condition on UTXD When set, a break condition will be asserted on the UTXD pin. A break condition is when the UTXD is driven low for more than one frame time (including Start, Parity, and Stop bits) measured at a give baud rate.
5	0	RW	URSPB UART Stick Parity Bit When set, the stick parity is enabled, ( stick parity has precedence over even/odd parity), i.e. if bit URPE, UREPb, and URSPB are all 1's, parity is always 0. If bits URPE, and URSPB are 1's, and bit UREPb is 0, parity is always 1. When reset, stick parity is disabled.
4	0	RW	UREPB UART Even Parity Bit 1 = even parity. 0 = odd parity.
3	0	RW	URPE UART Parity Enable (Even/Odd/Stick) When set, parity is enabled. When reset, parity is disabled.
2	0	RW	URSB UART Stop Bits 0 = 1 Stop bit per data frame. 1 = 2 Stop bit per data frame.
1:0	00	RW	URCL UART Character Length 00 = 5 data bits per frame. 01 = 6 data bits per frame. 10 = 7 data bits per frame.



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11 = 8 data bits per frame.

### 3.6.5 UART Modem Control Register (URMC Offset 0xE010)

The UART Modem Control register provides interface with the MODEM. All UART and Modem communication use software handshaking.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:5	0x0	RO	Reserved
4	0	RW	URLB UART Loop Back Mode When set, the UART is in the local loopback mode. This feature is for software diagnostics/testing. When reset, the UART is in normal functional mode. Note: In the UART loopback mode, the interrupt mechanism is fully operational. The operation of the Modem in the loopback mode is similar to external Modem loopback with Null modem cable.
3	0	RW	UROUT2 UART OUT2 When set, the internal UART OUT2 signal is asserted to 0. When reset, the internal UART OUT2 signal is deasserted.
2	0	RW	UROUT1 UART OUT1 When set, the internal UART OUT1 signal is asserted to 0. When reset, the internal UART OUT1 signal is deasserted.
1	0	RW	URRTS UART Request To Send When set, the UART RTS pin is asserted to 0. When reset, the UART RTS pin is deasserted.
0	0	RW	URDTR UART Data Terminal Ready When set, the UART DTR pin is asserted to 0. When reset, the UART DTR pin is deasserted.

### 3.6.6 UART Line Status Register (URLS Offset 0xE014)

The UART Line Status register provides status information to the CPU regarding the received data. The receive FIFO has 16 entries, each of which includes one byte of data and three error bits (parity error, framing error, and break interrupt) associated to the data. The Line status register is read only; writing to this register has no effect.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:8	0x0	RO	Reserved
7	0	RO	URRFE UART Receive FIFO Error This bit is meaningful only in FIFO mode to indicate that the UART receive FIFO contains error(s). Reading of '1' indicates there is at least one of the following errors: parity error, framing error, or break interrupt. This bit is cleared only when it is read by CPU and no subsequent errors in the FIFO.



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6	1	RO	<p>URTE UART Transmit Empty</p> <p>This bit indicates that the UART Transmit buffer is ready to accept new data for transmit.</p> <p>In character mode (16450):</p> <p>When set to '1', it indicates that the Transmit Holding Register and Transmitter Shift Register are both empty.</p> <p>In FIFO mode (16550):</p> <p>When set to '1', it indicates that both the Transmit FIFO and Transmitter Shift Register are empty</p>
5	1	RO	<p>URTHRE UART Transmit Holding Register Empty</p> <p>This bit indicates that the UART Transmit Holding Register (THR) is empty.</p> <p>In character mode (16450):</p> <p>When set to '1', it indicates the THR is empty.</p> <p>In FIFO mode (16550):</p> <p>When set to '1', it indicates that the Transmit FIFO is empty.</p>
4	0	RO	<p>URBI UART Break Interrupt Indicator</p> <p>In character mode (16450):</p> <p>When set, it indicates a "break" condition occurs on the URXD pin. A break condition is when the serial data is driven low for more than one frame time ( including Start, Parity, and Stop bits) measured at a give baud rate.</p> <p>In FIFO mode (16550):</p> <p>The break interrupt bit in the Receiver FIFO will be copied to this register bit when its associated character is at the top of the Receiver FIFO.</p> <p>This bit is reset to '0' when read.</p>
3	0	RO	<p>URFE UART Framing Error</p> <p>In character mode (16450):</p> <p>When set, the received character does not have the correct stop bit.( '0' is sampled)</p> <p>In FIFO mode (16550):</p> <p>The framing error bit in the Receiver FIFO will be copied to this register bit when its associated character is at the top of the Receiver FIFO.</p> <p>This bit reset to '0' when read.</p>
2	0	RO	<p>URPE UART Parity Error</p> <p>In character mode (16450):</p> <p>When set, the received character does not have the correct even or odd parity (excluding stick parity), as selected by the parity select bit.</p> <p>In FIFO mode (16550):</p> <p>The parity error bit in the Receiver FIFO will be copied to this register bit when its associated character is at the top of the Receiver FIFO.</p> <p>This bit reset to '0' when read.</p>
1	0	RO	<p>URROE UART Receive Overrun Error</p> <p>In character mode (16450):</p> <p>When set, the Receive Buffer Register (RBR) has not been read by the</p>



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			<p>CPU before the next character is ready to be transferred into RBR from the Receive Shift Register.</p> <p>In FIFO mode (16550):</p> <p>The Receiver FIFO is full and the next character is ready to be transferred into FIFO from the Receive Shift Register.</p> <p>This bit reset to '0' when read.</p>
0	0	RO	<p>URDR UART Receive Data Ready</p> <p>In character mode (16450):</p> <p>When set, data is valid in the Receive Buffer Register.</p> <p>In FIFO mode (16550):</p> <p>There is at least one character data ready in the Receive FIFO (not empty.)</p> <p>This bit will be cleared when no data in Receive Buffer Register or FIFO.</p>

### 3.6.7 UART Modem Status Register (URMS Offset 0xE018)

This register provides the current state of the Modem input control lines to the CPU. In addition to the current-state information, four bits of the Modem status register provide state-changing information. These bits are set to logic '1' whenever a control input from the remote Modem changes state. They are reset to '0' whenever the CPU reads the register. When either one of the four bits URLS[3:0] is set to '1', a Modem status interrupt is generated.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:8	0	RO	Reserved
7	--	RO	<p>URDCD UART Data Carrier Detect</p> <p>This bit indicates the logical (inverted) value of the UDCDN input.</p>
6	--	RO	<p>URRI UART Ring Indicator</p> <p>This bit indicates the logical (inverted) value of the URIN input pin.</p>
5	--	RO	<p>URDSR UART Data Set Ready</p> <p>This bit indicates the logical (inverted) value of the UDSRN input pin.</p>
4	--	RO	<p>URCTS UART Clear To Send</p> <p>This bit indicates the logical (inverted) value of the UCTSN input pin.</p>
3	0	RO	<p>URDDCD UART Delta Data Carrier Detect</p> <p>This bit is set when the UDCDN input pin has changed state.</p> <p>Cleared when read.</p>
2	0	RO	<p>URTERI UART Trailing Edge Ring Indicator</p> <p>This bit is set when the URIN input pin has changed from Low to High.</p> <p>Cleared when read.</p>
1	0	RO	<p>URDDST UART Delta Data Set Ready</p> <p>This bit is set when the UDSRN input pin has changed state.</p> <p>Cleared when read.</p>
0	0	RO	<p>URDCTS UART Delta Clear To Send</p> <p>This bit is set when the UCTSN input pin has changed state.</p>



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			Cleared when read.
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### 3.6.8 UART Baud Rate Divisor Register (URBD Offset 0xE01C)

The input clock to the baud rate generator is fixed at 25MHz. This clock is divided by the value in the URBD register to generate the sample clock (Fsample), which is used to sample the incoming data or to drive the outgoing data. The frequency of Fclk is 16 times of Fsample.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:24	0x0	RO	Reserved
23:0	0x1BE	RW	URBDC UART Baud Rate Divisor Count

### 3.6.9 UART Status Register (USR Offset 0xE020)

This register currently holds the Timeout Indication bit. The Timeout and Receive Triggered-level Reach shares the same interrupt Status(INTST[9]) bit. To further distinguish these two interrupt sources, a Timeout Indication bit is introduced.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:1	0x0	RO	Reserved
0	0	RO	UTI UART Timeout Indication bit If INTST[9] = 1 and USR[0] = 1, the interrupt source is from timeout. If INTST[9] = 1 and USR[0] = 0, the interrupt source is because the Receive FIFO has reached the trigger-level. Note that this bit will be automatically cleared when either a new coming frame has received or CPU reads Receive FIFO.

## 3.7 Interrupt Controller Registers

The KS8695PX supports multiple interrupt sources with configurable priority. Interrupt requests can be generated by internal functional blocks as well as external pins. The ARM core recognizes two kinds of interrupts: a normal interrupt request (IRQ), and a fast interrupt request (FIQ). All interrupts can be categorized as either IRQ or FIQ. The KS8695PX interrupt controller has an interrupt status bit for each interrupt source. This register defines the interrupt source for each device interrupt.

In general, four special registers are used to control interrupt generation and handling:

- Interrupt Mode Control Register: defines the interrupt source to the ARM core, IRQ or FIQ.
- Interrupt Priority Register: the index number of each interrupt source is written to the pre-defined interrupt priority register field to obtain the priority. The interrupt priorities are predefined from 0 to 15.
- Interrupt Status Register: indicates the interrupt status.
- Interrupt Enable Register: enables the interrupts.





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### 3.7.1 Interrupt Mode Control Register (INTMC Offset 0xE200)

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0	RW	WMLCIM WAN MAC Link Changed Interrupt Mode When set, the WAN MAC Link Change Interrupt corresponds to the FIQ (fast Interrupt). When reset, the WAN MAC Link Change Interrupt corresponds to the IRQ (normal interrupt).
30	0	RW	WMTIM WAN MAC Transmit Interrupt Mode When set, the WAN MAC Transmit Interrupt corresponds to the FIQ (fast Interrupt). When reset, the WAN MAC Transmit Interrupt corresponds to the IRQ (normal interrupt).
29	0	RW	WMRIM WAN MAC Receive Interrupt Mode When set, the WAN MAC Receive Interrupt corresponds to the FIQ (fast Interrupt). When reset, the WAN MAC Receive Interrupt corresponds to the IRQ (normal interrupt).
28	0	RW	WMTBUIM WAN MAC Transmit Buffer Unavailable Interrupt Mode When set, the WAN MAC Transmit Buffer Unavailable Interrupt corresponds to the FIQ (fast Interrupt). When reset, the WAN MAC Transmit Buffer Unavailable Interrupt corresponds to the IRQ (normal interrupt).
27	0	RW	WMRBUIM WAN MAC Receive Buffer Unavailable Interrupt Mode When set, the WAN MAC Receive Buffer Unavailable Interrupt corresponds to the FIQ (fast Interrupt). When reset, the WAN MAC Receive Buffer Unavailable Interrupt corresponds to the IRQ (normal interrupt).
26	0	RW	WMTPSIM WAN MAC Transmit Process Stopped Interrupt Mode When set, the WAN MAC Transmit Process Stopped Interrupt corresponds to the FIQ (fast interrupt). When reset, the WAN MAC Transmit Process Stopped Interrupt corresponds to the IRQ (normal interrupt).
25	0	RW	WMRPSIM WAN MAC Receive Process Stopped Interrupt Mode When set, the WAN MAC Receive Process Stopped Interrupt corresponds to the FIQ (fast interrupt). When reset, the WAN MAC Receive Process Stopped Interrupt corresponds to the IRQ (normal interrupt).
24	0	RW	ABERIM AMBA Bus Error Response Interrupt Mode When set, the AMBA Bus Error Response Interrupt corresponds to the FIQ (fast interrupt). When reset, the AMBA Bus Error Response Interrupt corresponds to the IRQ (normal interrupt).
23:18	0x0	RO	Reserved
17	0	RW	LMTIM LAN MAC Transmit Interrupt Mode



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			<p>When set, the LAN MAC Transmit Interrupt corresponds to the FIQ (fast Interrupt).</p> <p>When reset, the LAN MAC Transmit Interrupt corresponds to the IRQ (normal interrupt).</p>
16	0	RW	<p>LMRIM LAN MAC Receive Interrupt Mode</p> <p>When set, the LAN MAC Receive Interrupt corresponds to the FIQ (fast Interrupt).</p> <p>When reset, the LAN MAC Receive Interrupt corresponds to the IRQ (normal interrupt).</p>
15	0	RW	<p>LMTBUIM LAN MAC Transmit Buffer Unavailable Interrupt Mode</p> <p>When set, the LAN MAC Transmit Buffer Unavailable Interrupt corresponds to the FIQ (fast Interrupt).</p> <p>When reset, the LAN MAC Transmit Buffer Unavailable Interrupt corresponds to the IRQ (normal interrupt).</p>
14	0	RW	<p>LMRBUIM LAN MAC Receive Buffer Unavailable Interrupt Mode</p> <p>When set, the LAN MAC Receive Buffer Unavailable Interrupt corresponds to the FIQ (fast Interrupt).</p> <p>When reset, the LAN MAC Receive Buffer Unavailable Interrupt corresponds to the IRQ (normal interrupt).</p>
13	0	RW	<p>LMTPSIM LAN MAC Transmit Process Stopped Interrupt Mode</p> <p>When set, the LAN MAC Transmit Process Stopped Interrupt corresponds to the FIQ (fast interrupt).</p> <p>When reset, the LAN MAC Transmit Process Stopped Interrupt corresponds to the IRQ (normal interrupt).</p>
12	0	RW	<p>LMRPSIM LAN MAC Receive Process Stopped Interrupt Mode</p> <p>When set, the LAN MAC Receive Process Stopped Interrupt corresponds to the FIQ (fast interrupt).</p> <p>When reset, the LAN MAC Receive Process Stopped Interrupt corresponds to the IRQ (normal interrupt).</p>
11	0	RW	<p>MSIM Modem Status Interrupt Mode</p> <p>When set, the Modem status Interrupt corresponds to the FIQ (fast interrupt).</p> <p>When reset, the Modem status Interrupt corresponds to the IRQ (normal interrupt).</p> <p>Modem status is defined as logic OR of the following Modem conditions: Clear to Send, Data Set Ready, Ring Indicator, Data Carrier Detect.</p>
10	0	RW	<p>ULESM UART Line Error Status Mode</p> <p>When set, the UART Line Error Status Interrupt corresponds to the FIQ (fast interrupt).</p> <p>When reset, the UART Line Error Status Interrupt corresponds to the IRQ (normal interrupt).</p> <p>UART line error status is defined as logic OR of the following line conditions: Overrun Error, parity error, framing error, break interrupt.</p>
9	0	RW	<p>URIM UART Receive Interrupt Mode</p> <p>When set, the UART receive interrupt corresponds to the FIQ (fast interrupt).</p>



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			When reset, the UART receive interrupt corresponds to the IRQ (normal interrupt).
8	0	RW	UTIM UART Transmit Interrupt Mode When set, the UART transmit interrupt corresponds to the FIQ (fast interrupt). When reset, the UART transmit interrupt corresponds to the IRQ (normal interrupt).
7	0	RW	T1IM Timer 1 Interrupt Mode When set, the Timer 1 Interrupt corresponds to the FIQ (fast interrupt). When reset, the Timer 1 Interrupt corresponds to the IRQ (normal interrupt).
6	0	RW	T0IM Timer 0 Interrupt Mode When set, the Timer 0 Interrupt corresponds to the FIQ (fast interrupt). When reset, the Timer 0 Interrupt corresponds to the IRQ (normal interrupt).
5	0	RW	EXTI3M External Interrupt 3 Mode When set, the external interrupt 3 corresponds to the FIQ (fast interrupt). When reset, the external interrupt 3 corresponds to the IRQ (normal interrupt).
4	0	RW	EXTI2M External Interrupt 2 Mode When set, the external interrupt 2 corresponds to the FIQ (fast interrupt). When reset, the external interrupt 2 corresponds to the IRQ (normal interrupt).
3	0	RW	EXTI1M External Interrupt 1 Mode When set, the external interrupt 1 corresponds to the FIQ (fast interrupt). When reset, the external interrupt 1 corresponds to the IRQ (normal interrupt).
2	0	RW	EXTI0M External Interrupt 0 Mode When set, the external interrupt 0 corresponds to the FIQ (fast interrupt). When reset, the external interrupt 0 corresponds to the IRQ (normal interrupt).
1	0	RW	CCTM Communications Channel Transmit Mode When set, the communications channel transmit corresponds to the FIQ (fast interrupt). When reset, the communications channel transmit corresponds to the IRQ (normal interrupt).
0	0	RW	CCRM Communications Channel Receive Mode When set, the communications channel receive corresponds to the FIQ (fast interrupt). When reset, the communications channel receive corresponds to the IRQ (normal interrupt).



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### 3.7.2 Interrupt Enable Register (INTEN Offset 0xE204)

This register enables the interrupts from the internal or external sources.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0	RW	WMLCIE WAN MAC Link Changed Interrupt Enable When this bit is set, the WAN MAC Link Changed Interrupt is enabled. When this bit is reset, the WAN MAC Link Changed Interrupt is disabled.
30	0	RW	WMTIE WAN MAC Transmit Interrupt Enable When this bit is set, the WAN MAC Transmit Interrupt is enabled. When this bit is reset, the WAN MAC Transmit Interrupt is disabled.
29	0	RW	WMRIE WAN MAC Receive Interrupt Enable When this bit is set, the WAN MAC Receive Interrupt is enabled. When this bit is reset, the WAN MAC Receive Interrupt is disabled.
28	0	RW	WMTBUIE WAN MAC Transmit Buffer Unavailable Interrupt Enable When this bit is set, the WAN MAC Transmit Buffer Unavailable Interrupt is enabled. When this bit is reset, the WAN MAC Transmit Buffer Unavailable Interrupt is disabled.
27	0	RW	WMRBUIE WAN MAC Receive Buffer Unavailable Interrupt Enable When this bit is set, the WAN MAC Receive Buffer Unavailable Interrupt is enabled. When this bit is reset, the WAN MAC Receive Buffer Unavailable Interrupt is disabled.
26	0	RW	WMTPSIE WAN MAC Transmit Process Stopped Interrupt Enable When this bit is set, the WAN MAC Transmit Process Stopped Interrupt is enabled. When this bit is reset, the WAN MAC Transmit Process Stopped Interrupt is disabled.
25	0	RW	WMRPSIE WAN MAC Receive Process Stopped Interrupt Enable When this bit is set, the WAN MAC Receive Process Stopped Interrupt is enabled. When this bit is reset, the WAN MAC Receive Process Stopped Interrupt is disabled.
24	0	RW	ABERIE AMBA Bus Error Response Interrupt Enable When this bit is set, the AMBA Bus Error Response Interrupt is enabled. When this bit is reset, the AMBA Bus Error Response Interrupt is disabled.
23:18	0x0	RO	Reserved
17	0	RW	LMTIE LAN MAC Transmit Interrupt Enable When this bit is set, the LAN MAC Transmit Interrupt is enabled. When this bit is reset, the LAN MAC Transmit Interrupt is disabled.
16	0	RW	LMRIE LAN MAC Receive Interrupt Enable



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			When this bit is set, the LAN MAC Receive Interrupt is enabled. When this bit is reset, the LAN MAC Receive Interrupt is disabled.
15	0	RW	LMTBUIE LAN MAC Transmit Buffer Unavailable Interrupt Enable When this bit is set, the LAN MAC Transmit Buffer Unavailable Interrupt is enabled. When this bit is reset, the LAN MAC Transmit Buffer Unavailable Interrupt is disabled.
14	0	RW	LMRBUIE LAN MAC Receive Buffer Unavailable Interrupt Enable When this bit is set, the LAN MAC Receive Buffer Unavailable Interrupt is enabled. When this bit is reset, the LAN MAC Receive Buffer Unavailable Interrupt is disabled.
13	0	RW	LMTPSIE LAN MAC Transmit Process Stopped Interrupt Enable When this bit is set, the LAN MAC Transmit Process Stopped Interrupt is enabled. When this bit is reset, the LAN MAC Transmit Process Stopped Interrupt is disabled.
12	0	RW	LMRPSIE LAN MAC Receive Process Stopped Interrupt Enable When this bit is set, the LAN MAC Receive Process Stopped Interrupt is enabled. When this bit is reset, the LAN MAC Receive Process Stopped Interrupt is disabled.
11	0	RW	MSIE Modem Status Interrupt Enable When this bit is set, the Modem status Interrupt is enabled. When this bit is reset, the Modem status Interrupt is disabled. Modem status is defined as logic OR of the following Modem conditions: Clear to Send, Data Set Ready, Ring Indicator, Data Carrier Detect.
10	0	RW	ULESE UART Line Error Status Enable When this bit is set, the UART Line Error Status Interrupt is enabled. When this bit is reset, the UART Line Error Status Interrupt is disabled. UART line error status is defined as logic OR of the following line conditions: Overrun Error, parity error, framing error, break interrupt.
9	0	RW	URIE UART Receive Interrupt Enable When this bit is set, the UART receive interrupt is enabled. When this bit is reset, the UART receive interrupt is disabled.
8	0	RW	UTIE UART Transmit Interrupt Enable When this bit is set, the UART transmit interrupt is enabled. When this bit is reset, the UART transmit interrupt is disabled.
7	0	RW	T1IM Timer 1 Interrupt Enable When this bit is set, the Timer 1 Interrupt is enabled. When this bit is reset, the Timer 1 Interrupt is disabled.
6	0	RW	T0IM Timer 0 Interrupt Enable When this bit is set, the Timer 0 Interrupt is enabled. When this bit is reset, the Timer 0 Interrupt is disabled.



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5	0	RW	EXTI3 External Interrupt 3 Enable When this bit is set, the external interrupt 3 is enabled. When this bit is reset, the external interrupt 3 is disabled.
4	0	RW	EXTI2 External Interrupt 2 Enable When this bit is set, the external interrupt 2 is enabled. When this bit is reset, the external interrupt 2 is disabled.
3	0	RW	EXTI1 External Interrupt 1 Enable When this bit is set, the external interrupt 1 is enabled. When this bit is reset, the external interrupt 1 is disabled.
2	0	RW	EXTI0 External Interrupt 0 Enable When this bit is set, the external interrupt 0 is enabled. When this is reset, the external interrupt 0 is disabled.
1	0	RW	CCTE Communications Channel Transmit Enable When this bit is set, the Communications Channel Transmit is enabled. When this is reset, the Communications Channel Transmit is disabled.
0	0	RW	CCRE Communications Channel Receive Enable When this bit is set, the Communications Channel Receive is enabled. When this is reset, the Communications Channel Receive is disabled.

### 3.7.3 Interrupt Status Register (INTST Offset 0xE208)

This register contains all the status bits for the ARM CPU. When corresponding enable bit is set, it cause the CPU to be interrupted. This register is usually read by the driver during interrupt service routine or polling. The register bits are not cleared when read. Each field can be masked.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0	RW	WMLCS WAN MAC Link Changed Status When this bit is set, it indicates that the WAN MAC link status has changed from link up to link down or from link down to link up. This edge-triggered interrupt status is cleared by writing 1 to this bit.
30	0	RW	WMTS WAN MAC Transmit Status When this bit is set, it indicates that the WAN MAC has transmitted at least a frame on the WAN port and the MAC is ready for new frames from the host. This edge-triggered interrupt status is cleared by writing 1 to this bit.
29	0	RW	WMRS WAN MAC Receive Status When this bit is set, it indicates that the WAN MAC has received a frame from the WAN port and it is ready for the host to process This edge-triggered interrupt status is cleared by writing 1 to this bit.
28	0	RW	WMTBUS WAN MAC Transmit Buffer Unavailable Status When this bit is set, it indicates that the next descriptor on the transmit list is owned by the host and cannot be acquired by the KS8695PX. The transmission process is suspended. To resume processing transmit





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			<p>descriptors, the host should change the ownership bit of the descriptor and then issue a transmit start command.</p> <p>This edge-triggered interrupt status is cleared by writing 1 to this bit.</p>
27	0	RW	<p>WMRBUS WAN MAC Receive Buffer Unavailable Status</p> <p>When this bit is set, it indicates that the descriptor list is owned by the host and cannot be acquired by the KS8695PX. The receiving process is suspended. To resume processing receive descriptors, the host should change the ownership of the descriptor and may issue a receive start command. If no receive start command is issued, the receiving process resumes when the next recognized incoming frame is received. After the first assertion, this bit is not asserted for any subsequent not owned receive descriptors fetches. This bit is asserted only when the previous receive descriptor was owned by the KS8695PX.</p> <p>This edge-triggered interrupt status is cleared by writing 1 to this bit.</p>
26	0	RW	<p>WMT PSS WAN MAC Transmit Process Stopped Status</p> <p>Asserted when the WAN MAC transmit process enters the stopped state.</p> <p>This edge-triggered interrupt status is cleared by writing 1 to this bit.</p>
25	0	RW	<p>WMP PSS WAN MAC Receive Process Stopped Status</p> <p>Asserted when the WAN MAC receive process enters the stopped state.</p> <p>This edge-triggered interrupt status is cleared by writing 1 to this bit.</p>
24	0	RO	<p>ABERS AMBA Bus Error Response Status</p> <p>When this bit is set, it indicates that either WAN or LAN AMBA master has received a bus error response from slave(memory controller).</p> <p>This level-triggered interrupt status is automatically cleared when interrupt source is cleared.</p>
23:18	0x0	RO	Reserved
17	0	RW	<p>LMTS LAN MAC Transmit Status</p> <p>When this bit is set, it indicates that the LAN MAC has transmitted at least a frame on the LAN port and the MAC is ready for new frames from the host.</p> <p>This edge-triggered interrupt status is cleared by writing 1 to this bit.</p>
16	0	RW	<p>LMRS LAN MAC Receive Status</p> <p>When this bit is set, it indicates that the LAN MAC has received a frame from the LAN port and it is ready for the host to process</p> <p>This edge-triggered interrupt status is cleared by writing 1 to this bit.</p>
15	0	RW	<p>LMTBUS LAN MAC Transmit Buffer Unavailable Status</p> <p>When this bit is set, it indicates that the next descriptor on the transmit list is owned by the host and cannot be acquired by the KS8695PX. The transmission process is suspended. To resume processing transmit descriptors, the host should change the ownership bit of the descriptor and then issue a transmit start command.</p> <p>This edge-triggered interrupt status is cleared by writing 1 to this bit.</p>
14	0	RW	<p>LMRBUS LAN MAC Receive Buffer Unavailable Status</p> <p>When this bit is set, it indicates that the descriptor list is owned by the host and cannot be acquired by the KS8695PX. The receiving process is suspended. To resume processing receive descriptors, the host</p>



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			<p>should change the ownership of the descriptor and may issue a receive start command. If no receive start command is issued, the receiving process resumes when the next recognized incoming frame is received. After the first assertion, this bit is not asserted for any subsequent not owned receive descriptors fetches. This bit is asserted only when the previous receive descriptor was owned by the KS8695PX.</p> <p>This edge-triggered interrupt status is cleared by writing 1 to this bit.</p>
13	0	RW	<p>LMTPSS LAN MAC Transmit Process Stopped Status</p> <p>Asserted when the LAN MAC transmit process enters the stopped state.</p> <p>This edge-triggered interrupt status is cleared by writing 1 to this bit.</p>
12	0	RW	<p>LMRPSS LAN MAC Receive Process Stopped Status</p> <p>Asserted when the LAN MAC receive process enters the stopped state.</p> <p>This edge-triggered interrupt status is cleared by writing 1 to this bit.</p>
11	0	RO	<p>UMS UART Modem Status</p> <p>When this bit is set, it indicates that the UART modem status is set.</p> <p>UART modem status is defined as logic OR of Delta Data Carrier Detect, Trailing Edge Ring Indicator, Delta Data Set Ready and Delta Clear To Send.</p> <p>This level-triggered interrupt status is automatically cleared when UART Modem Status Register is read.</p>
10	0	RO	<p>ULES UART Line Error Status</p> <p>When this bit is set, it indicates that the UART line error status is set.</p> <p>UART line error status is defined as logic OR of the following line conditions:</p> <p>Overrun Error, parity error, framing error, break interrupt.</p> <p>This level-triggered interrupt status is automatically cleared when UART Line Status Register is read.</p>
9	0	RO	<p>URS UART Receive Status</p> <p>When this bit is set, it indicates that the UART receive status is set.</p> <p>UART receive status is defined as logic OR of received data available or character timeout indication.</p> <p>For received data available, it indicates Receive Buffer Register is full(character mode) or trigger-level reached(FIFO mode).</p> <p>This level-triggered interrupt status is automatically cleared when UART Receive Buffer Register is read or FIFO drops below trigger-level.</p> <p>For character timeout indication, it indicates timeout has occurred in FIFO mode.</p> <p>This level-triggered interrupt status is automatically cleared when CPU reads a datum back.</p> <p>Note that UART Status Register can provide further information if this interrupt status is for received data available or timeout.</p>
8	1	RW	<p>UTS UART Transmit Status</p> <p>When this bit is set, it indicates that the UART transmit status is set.</p> <p>UART transmit status is defined as the emptiness of Transmit Holding Register.</p> <p>This edge-triggered interrupt status is cleared by writing 1 to this bit.</p>
7	0	RW	<p>T1MS Timer 1 Status</p>





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			When this bit is set, it indicates that the Timer 1 status is set as specified in the Timer 1 registers. This edge-triggered interrupt status is cleared by writing 1 to this bit.
6	0	RW	T0MS Timer 0 Status When this bit is set, it indicates that the Timer 0 status is set as specified in the Timer 0 registers. This edge-triggered interrupt status is cleared by writing 1 to this bit.
5	0	RW	EXTI3S External Interrupt 3 Status When this bit is set, it indicates that the external interrupt 3 pin is set. This interrupt status is cleared by writing 1 to this bit if edge-trigger is selected.
4	0	RW	EXTI2S External Interrupt 2 Status When this bit is set, it indicates that the external interrupt 2 pin is set. This interrupt status is cleared by writing 1 to this bit if edge-trigger is selected.
3	0	RW	EXTI1S External Interrupt 1 Status When this bit is set, it indicates that the external interrupt 1 pin is set. This interrupt status is cleared by writing 1 to this bit if edge-trigger is selected.
2	0	RW	EXTI0S External Interrupt 0 Status When this bit is set, it indicates that the external interrupt 0 pin is set. This interrupt status is cleared by writing 1 to this bit if edge-trigger is selected.
1	0	RO	CCTS Communications Channel Transmit Status. When this bit is set, it indicates that the Communications Channel Transmit pin is set. When High, this signal denotes that the comms channel transmit buffer is empty. This level-triggered interrupt status is automatically cleared when interrupt source is cleared.
0	0	RO	CCRS Communications Channel Receive Status. When this bit is set, it indicates that the Communications Channel Receive pin is set. When High, this signal denotes that the comms channel receive buffer contains data waiting to be read by the processor core. This level-triggered interrupt status is automatically cleared when interrupt source is cleared.

#### 3.7.4 Interrupt Priority Register for WAN MAC (INTPW Offset 0xE20C)

This register configures the priority of the WAN DMA Interrupt sources. There are a total of 16 priority levels, 0xF has the highest priority; 0x0 has the lowest priority. Note that FIQ still has higher precedence over IRQ.



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The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:28	0x0	RW	WMRIP WAN MAC Link Changed Interrupt Priority Level This field defines the priority level of the WAN MAC Link Changed Interrupt if enabled.
27:24	0x0	RW	WMTIP WAN MAC Transmit Interrupt Priority Level This field defines the priority level of the WAN MAC Transmit Interrupt if enabled.
23:20	0x0	RW	WMRIP WAN MAC Receive Interrupt Priority Level This field defines the priority level of the WAN MAC Receive Interrupt if enabled.
19:16	0x0	RW	WMTBUIP WAN MAC Transmit Buffer Unavailable Interrupt Priority Level This field defines the priority level of the WAN MAC Transmit Buffer Unavailable Interrupt if enabled.
15:12	0x0	RW	WMTBUIP WAN MAC Receive Buffer Unavailable Interrupt Priority Level This field defines the priority level of the WAN MAC Receive Buffer Unavailable Interrupt if enabled.
11:8	0x0	RW	WMTIPSIP WAN MAC Transmit Process Stopped Interrupt Priority Level This field defines the priority level of the WAN MAC Transmit Process Stopped Interrupt if enabled.
7:4	0x0	RW	WMRPSIP WAN MAC Receive Process Stopped Interrupt Priority Level This field defines the priority level of the WAN MAC Receive Process Stopped Interrupt if enabled.
3:0	0x0	RO	Reserved

### 3.7.5 Interrupt Priority Register for LAN MAC (INTPL Offset 0xE214)

This register configures the priority of the LAN DMA Interrupt sources. There are a total of 16 priority levels, 0xF has the highest priority; 0x0 has the lowest priority. Note that FIQ still has higher precedence over IRQ.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:28	0x0	RW	Reserved.
27:24	0x0	RW	LMTIP LAN MAC Transmit Interrupt Priority Level This field defines the priority level of the LAN MAC Transmit Interrupt if enabled.
23:20	0x0	RW	LMRIP LAN MAC Receive Interrupt Priority Level This field defines the priority level of the LAN MAC Receive Interrupt if enabled.
19:16	0x0	RW	LMTBUIP LAN MAC Transmit Buffer Unavailable Interrupt Priority Level This field defines the priority level of the LAN MAC Transmit Buffer Unavailable Interrupt if enabled.



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15:12	0x0	RW	LMTBUIP LAN MAC Receive Buffer Unavailable Interrupt Priority Level This field defines the priority level of the LAN MAC Receive Buffer Unavailable Interrupt if enabled.
11:8	0x0	RW	LMTPSIP LAN MAC Transmit Process Stopped Interrupt Priority Level This field defines the priority level of the LAN MAC Transmit Process Stopped Interrupt if enabled.
7:4	0x0	RW	LMRPSIP LAN MAC Receive Process Stopped Interrupt Priority Level This field defines the priority level of the LAN MAC Receive Process Stopped Interrupt if enabled.
3:0	0x0	RO	Reserved

### 3.7.6 Interrupt Priority Register for Timer (INTPT Offset 0xE218)

This register configures the priority of the Timer Interrupt sources. There are a total of 16 priority levels, 0xF has the highest priority; 0x0 has the lowest priority. Note that FIQ still has higher precedence over IRQ.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:8	0x0	RO	Reserved
7:4	0x0	RW	T1IP Timer 1 Interrupt Priority Level This field defines the priority level of the Timer 1 Interrupt if enabled.
3:0	0x0	RW	T0IP Timer 0 Interrupt Priority Level This field defines the priority level of the Timer 0 Interrupt in enabled.

### 3.7.7 Interrupt Priority Register for UART (INTPU Offset 0xE21C)

This register configures the priority of the UART Interrupt sources. There are a total of 16 priority levels, 0xF has the highest priority; 0x0 has the lowest priority. Note that FIQ still has higher precedence over IRQ.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:16	0x0	RO	Reserved
15:12	0x0	RW	MSIP Modem Status Interrupt Priority Level This field defines the priority level of the Modem Status Interrupt if enabled.
11:8	0x0	RW	ULESIP UART Line Error Status Interrupt Priority Level This field defines the priority level of the Line Error Status Interrupt if enabled.
7:4	0x0	RW	URIP UART Receive Interrupt Priority Level This field defines the priority level of the UART Receive Interrupt if enabled.
3:0	0x0	RW	UTIP UART Transmit Interrupt Priority Level This field defines the priority level of the UART Transmit Interrupt if enabled.



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			enabled.
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### 3.7.8 Interrupt Priority Register for External Interrupt (INTPE Offset 0xE220)

This register configures the priority of the External Interrupt sources. There are a total of 16 priority levels, 0xF has the highest priority; 0x0 has the lowest priority. Note that FIQ still has higher precedence over IRQ.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:16	0x0	RO	Reserved
15:12	0x0	RW	EXTI3P External Interrupt 3 Priority Level This field defines the priority level of the External Interrupt 3 if enabled.
11:8	0x0	RW	EXTI2P External Interrupt 2 Priority Level This field defines the priority level of the External Interrupt 2 if enabled.
7:4	0x0	RW	EXTI1P External Interrupt 1 Priority Level This field defines the priority level of the External Interrupt 1 if enabled.
3:0	0x0	RW	EXTI0P External Interrupt 0 Priority Level This field defines the priority level of the External Interrupt 0 if enabled.

### 3.7.9 Interrupt Priority Register for Communications Channel (INTPC Offset 0xE224)

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:8	0x0	RO	Reserved
7:4	0x0	RW	CCTP Communications Channel Transmit Priority Level This field defines the priority level of the Communications Channel Transmit if enabled.
3:0	0x0	RW	CCRP Communications Channel Receive Priority Level This field defines the priority level of the Communications Channel Receive if enabled.

### 3.7.10 Interrupt Priority Register for Bus Error Response (INTPBE Offset 0xE228)

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:4	0x0	RO	Reserved
3:0	0x0	RW	ABERP AMBA Bus Error Response Priority Level This field defines the priority level of the Bus Error Response if enabled.

### 3.7.11 Interrupt Mask Status Register (INTMS Offset 0xE22C)

This register is the logical AND of the Interrupt Enable Register and the Interrupt Status Register. This register is read only.

The following table shows the register bit fields.



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BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0	RO	WMLCIMS WAN MAC Link Change Interrupt Mask Status When this bit is set, it indicates that the WAN MAC Link Change Interrupt is enabled and its corresponding status bit is set.
30	0	RO	WMTIMS WAN MAC Transmit Interrupt Mask Status When this bit is set, it indicates that the WAN MAC Transmit Interrupt is enabled and its corresponding status bit is set.
29	0	RO	WMRIMS WAN MAC Receive Interrupt Mask Status When this bit is set, it indicates that the WAN MAC Receive Interrupt is enabled and its corresponding status bit is set.
28	0	RO	WMTBUMS WAN MAC Transmit Buffer Unavailable Interrupt Mask Status When this bit is set, it indicates that the WAN MAC Transmit Buffer Unavailable Interrupt is enabled and its corresponding status bit is set.
27	0	RO	WMRBUMS WAN MAC Receive Buffer Unavailable Interrupt Mask Status When this bit is set, it indicates that the WAN MAC Receive Buffer Unavailable Interrupt is enabled and its corresponding status bit is set.
26	0	RO	WMTPSMS WAN MAC Transmit Process Stopped Interrupt Mask Status When this bit is set, it indicates that the WAN MAC Transmit Process Stopped Interrupt is enabled and its corresponding status bit is set.
25	0	RO	WMRPSMS WAN MAC Receive Process Stopped Interrupt Mask Status When this bit is set, it indicates that the WAN MAC Receive Process Stopped Interrupt is enabled and its corresponding status bit is set.
24	0	RO	ABERMS AMBA Bus Error Response Interrupt Mask Status When this bit is set, it indicates that the AMBA Bus Error Response Interrupt is enabled and its corresponding status bit is set.
23:18	0x00	RO	Reserved
17	0	RO	LMTIMS LAN MAC Transmit Interrupt Mask Status When this bit is set, it indicates that the LAN MAC Transmit Interrupt is enabled and its corresponding status bit is set.
16	0	RO	LMRIMS LAN MAC Receive Interrupt Mask Status When this bit is set, it indicates that the LAN MAC Receive Interrupt is enabled and its corresponding status bit is set.
15	0	RO	LMTBUMS LAN MAC Transmit Buffer Unavailable Interrupt Mask Status When this bit is set, it indicates that the LAN MAC Transmit Buffer Unavailable Interrupt is enabled and its corresponding status bit is set.
14	0	RO	LMRBUMS LAN MAC Receive Buffer Unavailable Interrupt Mask Status When this bit is set, it indicates that the LAN MAC Receive Buffer Unavailable Interrupt is enabled and its corresponding status bit is set.
13	0	RO	LMTPSMS LAN MAC Transmit Process Stopped Interrupt Mask Status When this bit is set, it indicates that the LAN MAC Transmit Process Stopped Interrupt is enabled and its corresponding status bit is set.



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12	0	RO	LMRPSMS LAN MAC Receive Process Stopped Interrupt Mask Status When this bit is set, it indicates that the LAN MAC Receive Process Stopped Interrupt is enabled and its corresponding status bit is set.
11	0	RO	MSIMS Modem Status Interrupt Mask Status When this bit is set, it indicates that the Modem status Interrupt is enabled and its corresponding status bit is set.
10	0	RO	ULEIMS UART Line Error Interrupt Mask Status When this bit is set, it indicates that the UART Line Error Status Interrupt is enabled and its corresponding status bit is set. UART line error status is defined as logic OR of the following line conditions: Overrun Error, parity error, framing error, break interrupt.
9	0	RO	URIMS UART Receive Interrupt Mask Status When this bit is set, it indicates that the UART receive interrupt is enabled and its corresponding status bit is set.
8	0	RO	UTIMS UART Transmit Interrupt Mask Status When this bit is set, it indicates that the UART transmit interrupt is enabled and its corresponding status bit is set.
7	0	RO	T1IMS Timer 1 Interrupt Mask Status When this bit is set, it indicates that the Timer 1 Interrupt is enabled and its corresponding status bit is set.
6	0	RO	T0IMS Timer 0 Interrupt Mask Status When this bit is set, it indicates that the Timer 0 Interrupt is enabled and its corresponding status bit is set.
5	0	RO	EXTI3MS External Interrupt 3 Mask Status When this bit is set, it indicates that the external interrupt 3 is enabled and its corresponding status bit is set.
4	0	RO	EXTI2MS External Interrupt 2 Mask Status When this bit is set, it indicates that the external interrupt 2 is enabled and its corresponding status bit is set.
3	0	RO	EXTI1MS External Interrupt 1 Mask Status When this bit is set, it indicates that the external interrupt 1 is enabled and its corresponding status bit is set.
2	0	RO	EXTI0MS External Interrupt 0 Mask Status When this bit is set, it indicates that the external interrupt 0 is enabled and its corresponding status bit is set.
1	0	RO	CCTMS Communications Channel Transmit Mask Status When this bit is set, it indicates that the Communications Channel Transmit is enabled and its corresponding status bit is set..
0	0	RO	CCRMS Communications Channel Receive Mask Status When this bit is set, it indicates that the Communications Channel Receive is enabled and its corresponding status bit is set..

### 3.7.12 Interrupt Pending Highest Priority Register for FIQ (INTHPF Offset 0xE230)



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This register provides the interrupt information for the host to identify the pending interrupts with highest priority for FIQ (fast interrupt). Note that it is possible to have more than one highest interrupts pending because of the same priority level. This register is provided to the host to quickly identify and service the FIQ interrupt with highest priority. This register is read only.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0	RO	WMLCIPF WAN MAC Link Changed Interrupt Pending for FIQ When this bit is set, it indicates that the WAN MAC Link Changed Interrupt has the highest priority among all the FIQ interrupts pending currently.
30	0	RO	WMTIPF WAN MAC Transmit Interrupt Pending for FIQ When this bit is set, it indicates that the WAN MAC Transmit Interrupt has the highest priority among all the FIQ interrupts pending currently.
29	0	RO	WMRIPF WAN MAC Receive Interrupt Pending for FIQ When this bit is set, it indicates that the WAN MAC Receive Interrupt has the highest priority among all the FIQ interrupts pending currently.
28	0	RO	WMTBUIPF WAN MAC Transmit Buffer Unavailable Interrupt Pending for FIQ When this bit is set, it indicates that the WAN MAC Transmit Buffer Unavailable Interrupt has the highest priority among all the FIQ interrupts pending currently.
27	0	RO	WMRBUIPF WAN MAC Receive Buffer Unavailable Interrupt Pending for FIQ When this bit is set, it indicates that the WAN MAC Receive Buffer Unavailable Interrupt has the highest priority among all the FIQ interrupts pending currently.
26	0	RO	WMTPSIPF WAN MAC Transmit Process Stopped Interrupt Pending for FIQ When this bit is set, it indicates that the WAN MAC Transmit Process Stopped Interrupt has the highest priority among all the FIQ interrupts pending currently.
25	0	RO	WMRPSIPF WAN MAC Receive Process Stopped Interrupt Pending for FIQ When this bit is set, it indicates that the WAN MAC Receive Process Stopped Interrupt has the highest priority among all the FIQ interrupts pending currently.
24	0	RO	ABERPF AMBA Bus Error Response Interrupt Pending for FIQ When this bit is set, it indicates that the AMBA Bus Error Response Interrupt has the highest priority among all the FIQ interrupts pending currently.
23:18	0x00	RO	Reserved
17	0	RO	LMTIPF LAN MAC Transmit Interrupt Pending for FIQ When this bit is set, it indicates that the LAN MAC Transmit Interrupt has the highest priority among all the FIQ interrupts pending currently.
16	0	RO	LMRIPF LAN MAC Receive Interrupt Pending for FIQ





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			When this bit is set, it indicates that the LAN MAC Receive Interrupt has the highest priority among all the FIQ interrupts pending currently.
15	0	RO	LMTBUIPF LAN MAC Transmit Buffer Unavailable Interrupt Pending for FIQ When this bit is set, it indicates that the LAN MAC Transmit Buffer Unavailable Interrupt has the highest priority among all the FIQ interrupts pending currently.
14	0	RO	LMRBUIPF LAN MAC Receive Buffer Unavailable Interrupt Pending for FIQ When this bit is set, it indicates that the LAN MAC Receive Buffer Unavailable Interrupt has the highest priority among all the FIQ interrupts pending currently.
13	0	RO	LMTPSIPF LAN MAC Transmit Process Stopped Interrupt Pending for FIQ When this bit is set, it indicates that the LAN MAC Transmit Process Stopped Interrupt has the highest priority among all the FIQ interrupts pending currently.
12	0	RO	LMRPSIPF LAN MAC Receive Process Stopped Interrupt Pending for FIQ When this bit is set, it indicates that the LAN MAC Receive Process Stopped Interrupt has the highest priority among all the FIQ interrupts pending currently.
11	0	RO	MSIPF Modem Status Interrupt Pending for FIQ When this bit is set, it indicates that the Modem status Interrupt has the highest priority among all the FIQ interrupts pending currently.
10	0	RO	ULEIPF UART Line Error Interrupt Pending for FIQ When this bit is set, it indicates that the UART Line Error Status Interrupt has the highest priority among all the FIQ interrupts pending currently.
9	0	RO	URIPF UART Receive Interrupt Pending for FIQ When this bit is set, it indicates that the UART receive interrupt has the highest priority among all the FIQ interrupts pending currently.
8	0	RO	UTIPF UART Transmit Interrupt Pending for FIQ When this bit is set, it indicates that the UART transmit interrupt has the highest priority among all the FIQ interrupts pending currently.
7	0	RO	T1IPF Timer 1 Interrupt Pending for FIQ When this bit is set, it indicates that the Timer 1 Interrupt has the highest priority among all the FIQ interrupts pending currently.
6	0	RO	T0IPF Timer 0 Interrupt Pending for FIQ When this bit is set, it indicates that the Timer 0 Interrupt has the highest priority among all the FIQ interrupts pending currently.
5	0	RO	EXTI3PF External Interrupt 3 Pending for FIQ When this bit is set, it indicates that the external interrupt 3 has the highest priority among all the FIQ interrupts pending currently.
4	0	RO	EXTI2PF External Interrupt 2 Pending for FIQ When this bit is set, it indicates that the external interrupt 2 has the



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			highest priority among all the FIQ interrupts pending currently.
3	0	RO	EXTI1PF External Interrupt 1 Pending for FIQ When this bit is set, it indicates that the external interrupt 1 has the highest priority among all the FIQ interrupts pending currently.
2	0	RO	EXTI0PF External Interrupt 0 Pending for FIQ When this bit is set, it indicates that the external interrupt 0 has the highest priority among all the FIQ interrupts pending currently.
1	0	RO	CCTPF Communications Channel Transmit Pending for FIQ When this bit is set, it indicates that the Communications Channel Transmit has the highest priority among all the FIQ interrupts pending currently..
0	0	RO	CCRPF Communications Channel Receive Pending for FIQ When this bit is set, it indicates that the Communications Channel Receive has the highest priority among all the FIQ interrupts pending currently..

#### 3.7.13 Interrupt Pending Highest Priority Register for IRQ (INTHPI Offset 0xE234)

This register provides the interrupt information for the host to identify the pending interrupts with highest priority for IRQ (normal interrupt) Note that it is possible to have more than one highest interrupts pending because of the same priority level. This register is provided to the host to quickly identify and service the IRQ interrupt with the highest priority. This register is read only.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0	RO	WMLCIPQ WAN MAC Link Changed Interrupt Pending for IRQ When this bit is set, it indicates that the WAN MAC Link Changed Interrupt has the highest priority among all the IRQ interrupts pending currently.
30	0	RO	WMTIPQ WAN MAC Transmit Interrupt Pending for IRQ When this bit is set, it indicates that the WAN MAC Transmit Interrupt has the highest priority among all the IRQ interrupts pending currently.
29	0	RO	WMRIPQ WAN MAC Receive Interrupt Pending for IRQ When this bit is set, it indicates that the WAN MAC Receive Interrupt has the highest priority among all the IRQ interrupts pending currently.
28	0	RO	WMTBUIPQ WAN MAC Transmit Buffer Unavailable Interrupt Pending for IRQ When this bit is set, it indicates that the WAN MAC Transmit Buffer Unavailable Interrupt has the highest priority among all the IRQ interrupts pending currently.
27	0	RO	WMRBUIPQ WAN MAC Receivet Buffer Unavailable Interrupt Pending for IRQ When this bit is set, it indicates that the WAN MAC Receive Buffer Unavailable Interrupt has the highest priority among all the IRQ interrupts pending currently.
26	0	RO	WMTPSIPQ WAN MAC Transmit Process Stopped Interrupt Pending for IRQ



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			When this bit is set, it indicates that the WAN MAC Transmit Process Stopped Interrupt has the highest priority among all the IRQ interrupts pending currently.
25	0	RO	WMRPSIPQ WAN MAC Receive Process Stopped Interrupt Pending for IRQ When this bit is set, it indicates that the WAN MAC Receive Process Stopped Interrupt has the highest priority among all the IRQ interrupts pending currently.
24	0	RO	ABERPF AMBA Bus Error Response Interrupt Pending for IRQ When this bit is set, it indicates that the AMBA Bus Error Response Interrupt has the highest priority among all the IRQ interrupts pending currently.
23:18	0x00	RO	Reserved
17	0	RO	LMTIPQ LAN MAC Transmit Interrupt Pending for IRQ When this bit is set, it indicates that the LAN MAC Transmit Interrupt has the highest priority among all the IRQ interrupts pending currently.
16	0	RO	LMRIPQ LAN MAC Receive Interrupt Pending for IRQ When this bit is set, it indicates that the LAN MAC Receive Interrupt has the highest priority among all the IRQ interrupts pending currently.
15	0	RO	LMTBUIPQ LAN MAC Transmit Buffer Unavailable Interrupt Pending for IRQ When this bit is set, it indicates that the LAN MAC Transmit Buffer Unavailable Interrupt has the highest priority among all the IRQ interrupts pending currently.
14	0	RO	LMRBUIPQ LAN MAC Receive Buffer Unavailable Interrupt Pending for IRQ When this bit is set, it indicates that the LAN MAC Receive Buffer Unavailable Interrupt has the highest priority among all the IRQ interrupts pending currently.
13	0	RO	LMTPSIPQ LAN MAC Transmit Process Stopped Interrupt Pending for IRQ When this bit is set, it indicates that the LAN MAC Transmit Process Stopped Interrupt has the highest priority among all the IRQ interrupts pending currently.
12	0	RO	LMRPSIPQ LAN MAC Receive Process Stopped Interrupt Pending for IRQ When this bit is set, it indicates that the LAN MAC Receive Process Stopped Interrupt has the highest priority among all the IRQ interrupts pending currently.
11	0	RO	MSIPQ Modem Status Interrupt Pending for IRQ When this bit is set, it indicates that the Modem status Interrupt has the highest priority among all the IRQ interrupts pending currently.
10	0	RO	ULEIPQ UART Line Error Interrupt Pending for IRQ When this bit is set, it indicates that the UART Line Error Status Interrupt has the highest priority among all the IRQ interrupts pending currently.
9	0	RO	URIPQ UART Receive Interrupt Pending for IRQ



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			When this bit is set, it indicates that the UART receive interrupt has the highest priority among all the IRQ interrupts pending currently.
8	0	RO	UTIPQ UART Transmit Interrupt Pending for IRQ When this bit is set, it indicates that the UART transmit interrupt has the highest priority among all the IRQ interrupts pending currently.
7	0	RO	T1IPQ Timer 1 Interrupt Pending for IRQ When this bit is set, it indicates that the Timer 1 Interrupt has the highest priority among all the IRQ interrupts pending currently.
6	0	RW	T0IPQ Timer 0 Interrupt Pending for IRQ When this bit is set, it indicates that the Timer 0 Interrupt has the highest priority among all the IRQ interrupts pending currently.
5	0	RO	EXTI3PQ External Interrupt 3 Pending for IRQ When this bit is set, it indicates that the external interrupt 3 has the highest priority among all the IRQ interrupts pending currently.
4	0	RO	EXTI2PQ External Interrupt 2 Pending for IRQ When this bit is set, it indicates that the external interrupt 2 has the highest priority among all the IRQ interrupts pending currently.
3	0	RO	EXTI1PQ External Interrupt 1 Pending for IRQ When this bit is set, it indicates that the external interrupt 1 has the highest priority among all the IRQ interrupts pending currently.
2	0	RO	EXTI0PQ External Interrupt 0 Pending for IRQ When this bit is set, it indicates that the external interrupt 0 has the highest priority among all the IRQ interrupts pending currently.
1	0	RO	CCTPQ Communications Channel Transmit Pending for IRQ When this bit is set, it indicates that the Communications Channel Transmit has the highest priority among all the IRQ interrupts pending currently.
0	0	RO	CCRPQ Communications Channel Receive Pending for IRQ When this bit is set, it indicates that the Communications Channel Receive has the highest priority among all the IRQ interrupts pending currently..

### 3.8 Timer Registers

#### 3.8.1 Timer Control Register (TMCON Offset 0xE400)

The KS8695PX has two 32-bit timers (Timer 0 and Timer 1). When the timer expires, it generates a pulse on the I/O pins. These timer can operate in a very flexible way. The host can control the timeout period as well as the pulse duration. The output signals are TOUT0 and TOUT1, respectively. These timers are enabled or disabled by this register. Interrupts can be generated by setting the corresponding interrupt control registers.

A timer generates a one-shot pulse with a preset timer clock duration whenever a timeout occurs. The duration of the one-shot pulse is also programmable by the host. This pulse consequently generates a time-out interrupt that is directly observable at the timer's configured output pin. The timer frequency is calculated as follows:

$$f_{TOUT} = f_{MCLK} / (\text{Timer data value} + \text{Pulse data value})$$



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When the timer is enabled, it loads a data value to its count register and begins decrementing the count register value. When the timer expires, the corresponding TOUT pin is then asserted. Then it loads the pulse count value into the count register and starts decrementing. When the pulse data count reaches zero, the associated interrupt is asserted ( if enabled ), the TOUT pin is deasserted, and the timer data value is reloaded again for the next timeout. This process repeats until the timer is disabled. In our design, the frequency of MCLK is 25MHz.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:2	0x0	RO	Reserved
1	0	RW	TOUT1E Timer 1 Enable When set, the timer 1 is enabled. Timer process starts as soon as this bit is set. Software should ensure correct timer count and pulse data values are preloaded before setting this bit.
0	0	RW	TOUT0E Timer 0 Enable When set, the timer 0 is enabled. Timer process starts as soon as this bit is set. Software should ensure correct timer count and pulse data values are preloaded before setting this bit.

#### 3.8.2 Timer 1 Timeout Count Register (T1TC Offset 0xE404)

This register controls the timeout count value to be preloaded to the down-counting register for Timer 1. Writing a zero to this register may result in unpredictable timer behavior.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	--	RW	TOUT1TC Timer 1 Timeout Count This field specifies the duration that the TOUT1 pin is Low in each timeout period. Writing zero to this register may cause unpredictable behavior.

#### 3.8.3 Timer 0 Timeout Count Register (T0TC Offset 0xE408)

This register controls the timeout count value to be preloaded to the down-counting register for Timer 0. Writing a zero to this register may result in unpredictable timer behavior.

Timer 0 can also be programmed as Watchdog timer when the Byte 0 of Timeout Count Register is programmed as 8'hFF. Once it has been programmed as a Watchdog timer, the value in Timeout Count Register can never be re-programmed unless the timer is disabled first. In normal system operation, the Watchdog timer will be periodically disabled by CPU before it expires. In case the Watchdog timer expires (indicating system gets hung and CPU can not periodically come in to clear the timer by clearing the timer enable bit), a reset signal (active high) will be generated to reset the whole system.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
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31:0	0xFFFF_FF00	RW	<p>TOUT0TC Timer 0 Timeout Count</p> <p>This field specifies the duration that the TOUT0 pin is Low in each timeout period. Writing zero to this register may cause unpredictable behavior.</p> <p>Note that if the lowest byte is configured as 8'hFF, Timer 0 becomes Watchdog Timer.</p>
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### 3.8.4 Timer 1 Pulse Count Register (T1PD Offset 0xE40C)

This register controls the pulse data value to be preloaded to the down-counting register for Timer 1. The TOUT1 pin output remains asserted at '1' until the pulse counter reaches zero. Writing a zero to this register may result in unpredictable timer behavior.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	--	RW	<p>TOUT1PC Timer 1 Pulse Count</p> <p>This field specifies the duration that the TOUT1 pin is High in each timeout period. Writing zero to this register may cause unpredictable behavior.</p>

### 3.8.5 Timer 0 Pulse Count Register (T0PD Offset 0xE410)

This register controls the pulse data value to be preloaded to the down-counting register for Timer 0. The TOUT0 pin output remains asserted at '1' until the pulse counter reaches zero. Writing a zero to this register may result in unpredictable timer behavior.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	--	RW	<p>TOUT0PC Timer 0 Pulse Count</p> <p>This field specifies the duration that the TOUT0 pin is High in each timeout period. Writing zero to this register may cause unpredictable behavior.</p>

## 3.9 GPIO Registers

### 3.9.1 I/O Port Mode Register (IOPM Offset 0xE600)

This register controls the I/O pin input output mode. Each I/O pin can be configured as Input or Output. Note that some of the I/O pins are shared with the external interrupts and timer output. When these pins are configured for timer output the I/O Port Mode configuration is overridden. If the pins shared with External Interrupt (GPIO pins 3 to 0) are configured as output pins and are enabled for External/Soft Interrupt (e.g. Port Control Register bit 15 is set to 1 enable the External/Soft Interrupt 3), the CPU can generate a soft interrupt by writing the appropriate data (based on the Trigger Mode defined in the Port Control Register) to the corresponding Port Data Register.

The following table shows the register bit fields.

BITS FIELD	DEFAULT	READ/	DESCRIPTION
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	VALUE	WRITE	
31:16	0x0	RO	Reserved
15	0	RW	IOPM15 I/O Port Mode for GPIO Pin 15 When set, the port is configured as an output pin. When reset, the port is configured as an input pin.
14	0	RW	IOPM14 I/O Port Mode for GPIO Pin 14 When set, the port is configured as an output pin. When reset, the port is configured as an input pin.
13	0	RW	IOPM13 I/O Port Mode for GPIO Pin 13 When set, the port is configured as an output pin. When reset, the port is configured as an input pin.
12	0	RW	IOPM12 I/O Port Mode for GPIO Pin 12 When set, the port is configured as an output pin. When reset, the port is configured as an input pin.
11	0	RW	IOPM11 I/O Port Mode for GPIO Pin 11 When set, the port is configured as an output pin. When reset, the port is configured as an input pin.
10	0	RW	IOPM10 I/O Port Mode for GPIO Pin 10 When set, the port is configured as an output pin. When reset, the port is configured as an input pin.
9	0	RW	IOPM9 I/O Port Mode for GPIO Pin 9 When set, the port is configured as an output pin. When reset, the port is configured as an input pin.
8	0	RW	IOPM8 I/O Port Mode for GPIO Pin 8 When set, the port is configured as an output pin. When reset, the port is configured as an input pin.
7	0	RW	IOPM7 I/O Port Mode for GPIO Pin 7 When set, the port is configured as an output pin. When reset, the port is configured as an input pin.
6	0	RW	IOPM6 I/O Port Mode for GPIO Pin 6 When set, the port is configured as an output pin. When reset, the port is configured as an input pin.
5	0	RW	IOPM5 I/O Port Mode for GPIO Pin 5 When set, the port is configured as an output pin. When reset, the port is configured as an input pin. Note that GPIO Pin 5 is shared with Timer 1 output.
4	0	RW	IOPM4 I/O Port Mode for GPIO Pin 4 When set, the port is configured as an output pin. When reset, the port is configured as an input pin. Note that GPIO Pin 4 is shared with Timer 0 output.
3	0	RW	IOPM3 I/O Port Mode for GPIO Pin 3 When set, the port is configured as an output pin. When reset, the port is configured as an input pin.





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			Note that GPIO Pin 3 is shared with External Interrupt 3 input.
2	0	RW	IOPM2 I/O Port Mode for GPIO Pin 2 When set, the port is configured as an output pin. When reset, the port is configured as an input pin. Note that GPIO Pin 2 is shared with External Interrupt 2 input.
1	0	RW	IOPM1 I/O Port Mode for GPIO Pin 1 When set, the port is configured as an output pin. When reset, the port is configured as an input pin. Note that GPIO Pin 1 is shared with External Interrupt 1 input.
0	0	RW	IOPM0 I/O Port Mode for GPIO Pin 0 When set, the port is configured as an output pin. When reset, the port is configured as an input pin. Note that GPIO Pin 0 is shared with External Interrupt 0 input.

### 3.9.2 I/O Port Control Register (IOPC Offset 0xE604)

This register controls the usage of the shared I/O pins.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:18	0x0	RO	Reserved
17	0	RW	IOTIM1EN GPIO Pin for Timer 1 Enable When set, the shared GPIO pin (TOUT1) for Timer 1 is used for the timer. When reset, the shared GPIO pin for Timer 1 is used for normal GPIO purpose.
16	0	RW	IOTIM0EN GPIO Pin for Timer 0 Enable When set, the shared GPIO pin (TOUT0) for Timer 0 is used for the timer. When reset, the shared GPIO pin for Timer 0 is used for normal GPIO operation.
15	0	RW	IOEINT3EN GPIO Pin for External/Soft Interrupt 3 Enable When set, the shared GPIO pin (EXT3) for external interrupt request 3 is used for the interrupt. When reset, the shared GPIO pin (EXT3) for external interrupt request 3 is used for normal GPIO operation.
14:12	000	RW	IOEINT3TM GPIO Pin for External/Soft Interrupt 3 Trigger Mode This field is used to configure the trigger mode for External Interrupt 3. 000= Level Detection (Active Low) 001= Level Detection (Active High) 01x= Rising Edge Detection 10x= Falling Edge Detection 11x= Both Edge Detection
11	0	RW	IOEINT2EN GPIO Pin for External/Soft Interrupt 2 Enable



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			When set, the shared GPIO pin (EXT2) for external interrupt request 2 is used for the interrupt. When reset, the shared GPIO pin (EXT2) for external interrupt request 2 is used for normal GPIO operation.
10:8	000	RW	IOEINT2TM GPIO Pin for External/Soft Interrupt 2 Trigger Mode This field is used to configure the trigger mode for External Interrupt 2. 000= Level Detection (Active Low) 001= Level Detection (Active High) 01x= Rising Edge Detection 10x= Falling Edge Detection 11x= Both Edge Detection
7	0	RW	IOEINT1EN GPIO Pin for External/Soft Interrupt 1 Enable When set, the shared GPIO pin (EXT1) for external interrupt request 1 is used for the interrupt. When reset, the shared GPIO pin (EXT1) for external interrupt request 1 is used for normal GPIO operation.
6:4	000	RW	IOEINT1TM GPIO Pin for External/Soft Interrupt 1 Trigger Mode This field is used to configure the trigger mode for External Interrupt 1. 000= Level Detection (Active Low) 001= Level Detection (Active High) 01x= Rising Edge Detection 10x= Falling Edge Detection 11x= Both Edge Detection
3	0	RW	IOEINT0EN GPIO Pin for External/Soft Interrupt 0 Enable When set, the shared GPIO pin (EXT0) for external interrupt request 0 is used for the interrupt. When reset, the shared GPIO pin (EXT0) for external interrupt request 0 is used for normal GPIO operation.
2:0	000	RW	IOEINT0TM GPIO Pin for External/Soft Interrupt 0 Trigger Mode This field is used to configure the trigger mode for External Interrupt 0. 000= Level Detection (Active Low) 001= Level Detection (Active High) 01x= Rising Edge Detection 10x= Falling Edge Detection 11x= Both Edge Detection

### 3.9.3 I/O Port Data Register (IOPD Offset 0xE608)

This register contains the one-bit read values for I/O ports that are configured as input port, and one-bit write value for I/O ports that are configured as output port. Bits[15:0] of the 16-bit I/O port register value correspond directly to the 16 I/O pins, GPIO[15:0].

The following table shows the register bit fields.



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BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:16	0x0	RO	Reserved
15:0	--	RW	IOPD I/O Port Data Value The values reflect the signal level on the respective I/O port pins. When the ports are configured as output port, the bit reflects the port write value. When the port is configured as input port, the bit reflects the port read value.

### 3.10 Switch Engine Registers

Note 1: unless otherwise specified,

1 = feature enabled,

0 = feature disabled

#### 3.10.1 Switch Engine Control 0 Register (SEC0 Offset 0xE800)

The following table shows the register bit fields. Default: 0x4081\_9E00

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0	RW	New Backoff Enable =1, New backoff algorithm design for UNH
30:28	0x4	RW	802.1p base priority Used to classify priority for incoming 802.1Q packets. "user priority" is compared against this value. >= : classified as high priority < : classified as low priority
27:25	0x0	RW	LLED1S LAN LED1 Select 000: Speed 001: Link 010: Full Duplex 011: Collision 100: TX/RX Activities 101: Full Duplex/ Collision 110: Link/ Activities
24:22	0x2	RW	LLED0S LAN LED0 Select 000: Speed 001: Link 010: Full Duplex 011: Collision 100: TX/RX Activities 101: Full Duplex/ Collision 110: Link/ Activities
21	0	RW	UNH mode =1 the switch will drop packets with 0x8808 in T/L filed, or DA = 01-80-C2-00-00-01 =0, the switch will drop packets qualified as "flow control" packets.
20	0	RW	Link Change Age



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			=1, link change from "link" to "no link" will cause fast aging (<800us) to age address table faster. After an age cycle is complete, the age logic will return to normal (300 ± 75 seconds ). Note: If any port is unplugged, all addresses will be automatically aged out.
19	0	RW	Pass all frames =1, switch all packets including bad ones. Used solely for debugging purpose. Works in conjunction with Sniffer mode.
18	0	RW	Switch MII flow control enable =1, enable full duplex flow control on Switch MII interface. =0, disable full duplex flow control on Switch MII interface.
17	0	RW	Frame Length Field Check 1, Will check frame length field in the IEEE packets. If the actual length does not match, the packet will be dropped (for < 1500).
16	1	RW	Buffer share mode =1, buffer pool is shared by all ports. A port can use more buffer when other ports are not busy. =0, a port is only allowed to use 1/5 of the buffer pool
15	1	RW	Aging enable 1=Enable age function in the chip
14	0	RW	Enable fast aging 1=Turn on fast age (800us)
13	0	RW	Aggressive back off enable 1=Enable more aggressive back off algorithm in half duplex mode to enhance performance. This is not an IEEE standard
12	1	RW	Unicast port-VLAN mismatch discard This feature is used for port-VLAN (described in SEAFC and SEP1-5C) =1, all packets can not cross VLAN boundary =0, unicast packets (excluding unknown/multicast/broadcast) can cross VLAN boundary
11	1	RW	Multicast Storm Protection Disable =1, "Broadcast Storm Protection" does not include multicast packets. Only DA=FFFFFFFFFFFFFF packets will be regulated. =0, "Broadcast Storm Protection" includes DA =FFFFFFFFFFFFFF and DA[40] = 1 packets.
10	1	RW	Backpressure mode. =1, carrier sense based backpressure is selected. =0, collision based backpressure is selected.
9	1	RW	Flow control and back pressure fair mode. =1, fair mode is selected. In this mode, if a flow control port and a non flow control port talk to the same destination port, packets from the non flow control port may be dropped. This is to prevent the flow control port from being flow controlled for an extended period of time. =0, in this mode, if a flow control port and a non-flow control port talk to the same destination port, the flow control port will be flow controlled. This may not be "fair" to the flow control port.
8	0	RW	No excessive collision drop =1, the switch will not drop packets when 16 or more collisions occur. =0, the switch will drop packets when 16 or more collisions occur.
7	0	RW	Legal Maximum Packet size check disable =1, will accept packet sizes up to 1536 bytes (inclusive).



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			=0, 1522 bytes for tagged packets, 1518 bytes for untagged packets. Any packets larger than the specified value will be dropped.
6	0	RW	Priority Buffer reserve =1, Each output queue is pre-allocated 48 buffers, used exclusively for high priority packets. It is recommended to enable this when priority queue feature is turned on. =0, No reserved buffers for high priority packets.
5	0	RW	Switch MII back pressure enable 1, enable half duplex back pressure on switch MII interface. 0, disable back pressure on switch MII interface
4	0	RW	Switch MII half duplex mode 1, enable MII interface half duplex mode. 0, enable MII interface full duplex mode.
3:2	0x0	RW	Priority scheme select: 00 = always deliver high priority packets first 01 = deliver high/low packets at ratio 10/1 10 = deliver high/low packets at ratio 5/1 11 = deliver high/low packets at ratio 2/1
1	0	RW	Enable "tag" mask 1, the last 5 digits in the VID field are used as a mask to determine which port(s) the packet should be forwarded to. 0, no tag masks.
0	0	RW	Enable switch function. 1, switch enabled to receive and transmit. 0, no packets will be received or transmitted.

#### 3.10.2 Switch Engine Control 1 Register (SEC1 Offset 0xE804)

The following table shows the register bit fields. Default: 0x0940\_0100

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:21	0x04A	RW	Byte count [10:0] used for broadcast storm protection. Determines how many "64 byte blocks" of packet data allowed on an input port in a preset period: 50ms for 100BT 500ms for 10BT. The default is 1%.
20:13	0x00		Reserved
12	0	RW	Reserved. For testing purposes only.
11	0	RW	Non-IEEE Specification auto-negotiation = 0, don't follow IEEE specification for auto-negotiation = 1, follow IEEE specification for auto-negotiation
10	0	RW	Special TPID mode Used for direct mode forwarding from port 5. See description in "spanning tree" functional description.
9	0		Reserved
8	1	RW	Enable PHY MII 1, enable PHY MII interface (note: if not enabled, the switch will tri-state all outputs).



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7	0	RW	IEEE 802.1x Transmit flow control disable =0, will enable transmit flow control based on AN result. =1, will not enable transmit flow control regardless of AN result
6	0	RW	IEEE 802.1x Receive flow control disable =0, will enable receive flow control based on AN result. =1, will not enable receive flow control regardless of AN result
5	0	RW	Huge packet support =1, will accept packet sizes up to 1916 bytes (inclusive). This bit setting will override setting from bit 1 of the same register. =0, the max packet size will be determined by bit 1 of this register.
4	0	RW	802.1Q VLAN enable 1, Each output queue is pre-allocated 48 buffers, used exclusively for high priority packets. It is recommended to enable this when priority queue feature is turned on. 0, No reserved buffers for high priority packets.
3:2	00		Reserved.
1	0	RW	Switch MII 10BT =1, the switch interface is in 10Mbps mode =0, the switch interface is in 100Mbps mode
0	0	RW	Null VID replacement =1, will replace NULL VID with port VID(12 bits) =0, no replacement for NULL VID

### 3.10.3 Switch Engine Control 2 Register (SEC2 Offset 0xE808)

The following table shows the register bit fields. Default: 0x0024\_2424

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:24	0x00		Reserved
23:0	0x242424	RO	Factory default. Do not change.

### 3.10.4 Port 1-4 Config Regs (SEP1C1-SEP4C1 Offsets 0xE80C, 0xE818, 0xE824, 0xE830)

**Port 1 Configuration Register 1 (SEP1C1 Offset 0xE80C)**

**Port 2 Configuration Register 1 (SEP2C1 Offset 0xE818)**

**Port 3 Configuration Register 1 (SEP3C1 Offset 0xE824)**

**Port 4 Configuration Register 1 (SEP4C1 Offset 0xE830)**

The following table shows the register bit fields. Default: 0x0000\_5FC0

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:16	0x0000	RW	Port's default tag value for the port (ingress). 31:29 – user priority bits 28 – CFI bit 27:16 – VID[11:0]
15	0	RW	Disable auto negotiation. 1, disable auto negotiation, speed and duplex are specified by bits 14:13 respectively of this register.
14	1	RW	Forced speed



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			1, force 100BT when auto negotiation is disabled (bit15). 0, force 10BT when auto negotiation is disabled (bit15).
13	0	RW	Forced duplex. 1, full duplex when auto negotiation is disabled (bit15). 0, half duplex when auto negotiation is disabled (bit15).
12:8	0x1F	RW	Define the port's "port VLAN membership". Bit 12 indicates port 5, bit 11 indicates port 4, ..., bit 8 indicates port 1. The port can only communicate within the membership. A "1" includes a port in the membership, a "0" excludes a port from membership.
7	1	RW	Spanning Tree transmit enable on the port, BPDU excluded. 1, enable packet transmission on the port. 0, disable packet transmission on the port.
6	1	RW	Spanning Tree receive enable on the port, BPDU excluded. 1, enable packet reception on the port. 0, disable packet reception on the port.
5	0	RW	Spanning Tree learning disable on the port. 1, disable switch address learning capability. 0, enable switch address learning capability.
4	0	RW	Broadcast Storm protection on the port. 1, enable broadcast storm protection for ingress packets on the port. 0, disable broadcast storm protection.
3	0	RW	Port based priority classification enable. 1, ingress packets on the port will be classified as high priority if "Diffserv" or "802.1p" classification is not enabled or fails to classify. 0, ingress packets on port will be classified as low priority if "Diffserv" or "802.1p" classification is not enabled or fails to classify. Note: "Diffserv", "802.1p" and port priority can be enabled at the same time. The OR'ed result of 802.1p and DSCP overwrites the port priority.
2	0	RW	Diffserv priority classification enable 1, enable diffserv priority classification for ingress packets on port 0, disable diffserv function.
1	0	RW	802.1p based priority classification enable 1, enable 802.1p priority classification for ingress packets on port 0, disable 802.1p
0	0	RW	Enable priority function on the port 1, the port output queue is split into high and low priority queues. 0, single output queue on the port. There is no priority differentiation even though packets are classified into high or low priority.

#### 3.10.5 Port 1-4 Config Regs (SEP1C2-SEP4C2 Offsets 0xE810, 0xE81C, 0xE828, 0xE834)

**Port 1 Configuration Register 2 (SEP1C2 Offset 0xE810)**

**Port 2 Configuration Register 2 (SEP2C2 Offset 0xE81C)**

**Port 3 Configuration Register 2 (SEP3C2 Offset 0xE828)**

**Port 4 Configuration Register 2 (SEP4C2 Offset 0xE834)**

The following table shows the register bit fields. Default: 0x0000\_0000





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BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:29	0x0		Reserved
28	0	RW	Ingress VLAN filtering =1, the switch will discard packets whose VID port membership in VLAN table bit[20:16] does not include the ingress port. =0, no ingress VLAN filtering
27	0	RW	Discard Non PVID packets =1, the switch will discard packets whose VID does not match ingress port default VID. =0, no packets will be discarded
26	0	RW	Force flow control =1, will always enable rx and tx flow control on the port, regardless of AN result.  =0, the flow control is enabled based on AN result. Note: Setting a port for both half duplex and forced flow control is an illegal configuration. For half duplex enable back pressure.
25	0	RW	Back pressure enable =1, enable port's half duplex back pressure =0, disable port's half duplex back pressure.
24	0	RW	For test purposes only.
23:12	0x000	RW	Transmit high priority rate control. Determines how many "32Kbps" high priority blocks can be transmitted (in units of 4K bytes in a one second period).
11:0	0x000	RW	Transmit low priority rate control. Determines how many "32Kbps" low priority blocks can be transmitted (in units of 4K bytes in a one second period).

### 3.10.6 Port 1-4 Config Regs (SEP1C3-SEP4C3 Offsets 0xE814, 0xE820, 0xE82C, 0xE838)

**Port 1 Configuration Register 3 (SEP2C3 Offset 0xE814)**

**Port 2 Configuration Register 3 (SEP2C3 Offset 0xE820)**

**Port 3 Configuration Register 3 (SEP3C3 Offset 0xE82C)**

**Port 4 Configuration Register 3 (SEP4C3 Offset 0xE838)**

The following table shows the register bit fields. Default: 0x0000\_0000

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:20	0x000	RW	Receive high priority rate control. Determines how many "32Kbps" high priority blocks can be received (in units of 4K bytes in a one second period).
19:8	0x000	RW	Receive low priority rate control. Determines how many "32Kbps" low priority blocks can be received (in units of 4K bytes in a one second period).
7	0	RW	Receive differential priority rate control. 1, if bit 6 is also "1", this will enable receive rate control for this port on low priority packets at the low priority rate. If bit 5 is also "1", this will



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			enable receive rate control on high priority packets at the high priority rate. 0, receive rate control will be based on the low priority rate for all packets on this port.
6	0	RW	Low priority receive rate control enable. 1, enable port's low priority receive rate control feature. 0, disable port's low priority receive rate control feature.
5	0	RW	High priority receive rate control enable. 1, if bit 7 is also "1" this will enable the port's high priority receive rate control feature. If bit 7 is a "0" and bit 6 is a "1", all receive packets on this port will be rate controlled at the low priority rate. 0, disable port's high priority receive rate control feature.
4	0	RW	Low priority receive rate flow control enable. 1, flow control may be asserted if the port's low priority receive rate is exceeded. 0, flow control is not asserted if the port's low priority receive rate is exceeded.
3	0	RW	High priority receive rate flow control enable. 1, flow control may be asserted if the port's high priority receive rate is exceeded. 0, flow control is not asserted if the port's high priority receive rate is exceeded.
2	0	RW	Transmit differential priority rate control. 1, will do transmit rate control on both high and low priority packets based on the rate counters defined by the high and low priority packets, respectively.. 0, will do transmit rate control on any packets. The rate counters defined in low priority will be used..
1	0	RW	Low priority transmit rate control enable. 1, enable port's low priority transmit rate control feature. 0, disable port's low priority transmit rate control feature.
0	0	RW	High priority transmit rate control enable. 1, enable port's high priority transmit rate control feature. 0, disable port's high priority transmit rate control feature.

#### 3.10.7 Port 5 Configuration Register (SEP5C1 Offset 0xE83C)

The following table shows the register bit fields. Default: 0x0000\_1FC0

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:16	0x0000	RW	Port's default tag value for the port (ingress). 31:29 – user priority bits



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			28 – CFI bit 27:16 – VID[11:0]
15:13	0		Reserved.
12:8	0x1F	RW	Define the port's "port VLAN membership". Bit 12 indicates port 5, bit 11 indicates port 4, ..., bit 8 indicates port 1. The port can only communicate within the membership. A "1" includes a port in the membership, a "0" excludes a port from membership.
7	1	RW	Spanning Tree transmit enable on the port, BPDU excluded. 1, enable packet transmission on the port. 0, disable packet transmission on the port.
6	1	RW	Spanning Tree receive enable on the port, BPDU excluded. 1, enable packet reception on the port. 0, disable packet reception on the port.
5	0	RW	Spanning Tree learning disable on the port. 1, disable switch address learning capability. 0, enable switch address learning capability.
4	0	RW	Broadcast Storm protection on the port. 1, enable broadcast storm protection for ingress packets on the port. 0, disable broadcast storm protection.
3	0	RW	Port based priority classification enable. 1, ingress packets on the port will be classified as high priority if "Diffserv" or "802.1p" classification is not enabled or fails to classify. 0, ingress packets on port will be classified as low priority if "Diffserv" or "802.1p" classification is not enabled or fails to classify. Note: "Diffserv", "802.1p" and port priority can be enabled at the same time. The OR'ed result of 802.1p and DSCP overwrites the port priority.
2	0	RW	Diffserv priority classification enable 1, enable diffserv priority classification for ingress packets on port 0, disable diffserv function.
1	0	RW	802.1p based priority classification enable 1, enable 802.1p priority classification for ingress packets on port 0, disable 802.1p
0	0	RW	Enable priority function on the port 1, the port output queue is split into high and low priority queues. 0, single output queue on the port. There is no priority differentiation even though packets are classified into high or low priority.

### 3.10.8 Port 5 Configuration Register (SEP5C2 Offset 0xE840)

The following table shows the register bit fields. Default: 0x0000\_0000

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:29	0x0		Reserved
28	0	RW	Ingress VLAN filtering



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			=1, the switch will discard packets whose VID port membership in VLAN table bit[20:16] does not include the ingress port. =0, no ingress VLAN filtering
27	0	RW	Discard Non PVID packets =1, the switch will discard packets whose VID does not match ingress port default VID. =0, no packets will be discarded
26	0	RW	Force flow control =1, will always enable rx and tx flow control on the port, regardless of AN result.  =0, the flow control is enabled based on AN result. Note: Setting a port for both half duplex and forced flow control is an illegal configuration. For half duplex enable back pressure.
25	0	RW	Back pressure enable =1, enable port's half duplex back pressure =0, disable port's half duplex back pressure.
24	0		For test purpose only.
23:12	0x000	RW	Transmit high priority rate control. Determines how many "32Kbps" high priority blocks can be transmitted (in units of 4K bytes in a one second period).
11:0	0x000	RW	Transmit low priority rate control. Determines how many "32Kbps" low priority blocks can be transmitted (in units of 4K bytes in a one second period).

### 3.10.9 Port 5 Configuration Register (SEP5C3 Offset 0xE844)

The following table shows the register bit fields. Default: 0x0000\_0000

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:20	0x000	RW	Receive high priority rate control. Determines how many "32Kbps" high priority blocks can be received (in units of 4K bytes in a one second period).
19:8	0x000	RW	Receive low priority rate control. Determines how many "32Kbps" low priority blocks can be received (in units of 4K bytes in a one second period).
7	0	RW	Receive differential priority rate control. 1, if bit 6 is also "1", this will enable receive rate control for this port on low priority packets at the low priority rate. If bit 5 is also "1", this will enable receive rate control on high priority packets at the high priority rate. 0, receive rate control will be based on the low priority rate for all packets on this port.
6	0	RW	Low priority receive rate control enable. 1, enable port's low priority receive rate control feature. 0, disable port's low priority receive rate control feature.
5	0	RW	High priority receive rate control enable.



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			<p>1, if bit 7 is also "1" this will enable the port's high priority receive rate control feature. If bit 7 is a "0" and bit 6 is a "1", all receive packets on this port will be rate controlled at the low priority rate.</p> <p>0, disable port's high priority receive rate control feature.</p>
4	0	RW	<p>Low priority receive rate flow control enable.</p> <p>1, flow control may be asserted if the port's low priority receive rate is exceeded.</p> <p>0, flow control is not asserted if the port's low priority receive rate is exceeded.</p>
3	0	RW	<p>High priority receive rate flow control enable.</p> <p>1, flow control may be asserted if the port's high priority receive rate is exceeded.</p> <p>0, flow control is not asserted if the port's high priority receive rate is exceeded.</p>
2	0	RW	<p>Transmit differential priority rate control.</p> <p>1, will do transmit rate control on both high and low priority packets based on the rate counters defined by the high and low priority packets, respectively..</p> <p>0, will do transmit rate control on any packets. The rate counters defined in low priority will be used..</p>
1	0	RW	<p>Low priority transmit rate control enable.</p> <p>1, enable port's low priority transmit rate control feature.</p> <p>0, disable port's low priority transmit rate control feature.</p>
0	0	RW	<p>High priority transmit rate control enable.</p> <p>1, enable port's high priority transmit rate control feature.</p> <p>0, disable port's high priority transmit rate control feature.</p>

#### 3.10.10 Ports 1 & 2 Auto Negotiation (AN) Register (SEP12AN Offset 0xE848)

The following table shows the register bit fields. Default: 0x1F00\_1F00

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0		Reserved
30	0	RO	Port 1 AN complete. =1, AN done =0, AN not done
29	0	RW	Port 1 AN restart (self clearing). =1, restart auto-negotiation =0, normal operation
28	1	RW	Port 1 AN advertise flow control capability =1, advertise flow control capability =0, suppress flow control capability from transmission to link partner
27	1	RW	Port 1 AN advertise 100 Full Duplex. =1, advertise 100BT Full duplex capability =0, suppress 100BT Full duplex capability from transmission to link partner
26	1	RW	Port 1 AN advertise 100 Half Duplex. =1, advertise 100BT half duplex capability



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			=0, suppress 100BT half duplex capability from transmission to link partner
25	1	RW	Port 1 AN advertise 10 Full Duplex. =1, advertise 10BT Full duplex capability =0, suppress 10BT Full duplex capability from transmission to link partner
24	1	RW	Port 1 AN advertise 10 Half Duplex. =1, advertise 10BT Half duplex capability =0, suppress 10BT Half duplex capability from transmission to link partner
23	0	RO	Port 1 Link status. =1, Link good =0, Link not good
22	0	RO	Port 1 duplex status (resolved).
21	0	RO	Port 1 speed status (resolved).
20	0	RO	Port 1 Link Partner flow Control capability =1, link partner flow control capable =0, link partner not flow control capable
19	0	RO	Port 1 Link Partner 100 Full Duplex capability =1, link partner 100BT full duplex capable =0, link partner not 100BT full duplex capable
18	0	RO	Port 1 Link Partner 100 Half Duplex capability =1, link partner 100BT half duplex capable =0, link partner not 100BT half duplex capable
17	0	RO	Port 1 Link Partner 10 Full Duplex capability =1, link partner 10BT full duplex capable =0, link partner not 10BT full duplex capable
16	0	RO	Port 1 Link Partner 10 Half Duplex capability =1, link partner 10BT half duplex capable =0, link partner not 10BT half duplex capable
15	0		Reserved
14	0	RO	Port 2 AN complete. =1, AN done =0, AN not done
13	0	RW	Port 2 AN restart (self clearing). =1, restart auto-negotiation =0, normal operation
12	1	RW	Port 2 AN advertise flow control capability =1, advertise flow control capability =0, suppress flow control capability from transmission to link partner
11	1	RW	Port 2 AN advertise 100 Full Duplex. =1, advertise 100BT Full duplex capability =0, suppress 100BT Full duplex capability from transmission to link partner
10	1	RW	Port 2 AN advertise 100 Half Duplex. =1, advertise 100BT half duplex capability =0, suppress 100BT half duplex capability from transmission to link partner



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9	1	RW	Port 2 AN advertise 10 Full Duplex. =1, advertise 10BT Full duplex capability =0, suppress 10BT Full duplex capability from transmission to link partner
8	1	RW	Port 2 AN advertise 10 Half Duplex. =1, advertise 10BT Half duplex capability =0, suppress 10BT Half duplex capability from transmission to link partner
7	0	RO	Port 2 Link status. =1, Link good =0, Link not good
6	0	RO	Port 2 duplex status (resolved).
5	0	RO	Port 2 speed status (resolved).
4	0	RO	Port 2 Link Partner flow Control capability =1, link partner flow control capable =0, link partner not flow control capable
3	0	RO	Port 2 Link Partner 100 Full Duplex capability =1, link partner 100BT full duplex capable =0, link partner not 100BT full duplex capable
2	0	RO	Port 2 Link Partner 100 Half Duplex capability =1, link partner 100BT half duplex capable =0, link partner not 100BT half duplex capable
1	0	RO	Port 2 Link Partner 10 Full Duplex capability =1, link partner 10BT full duplex capable =0, link partner not 10BT full duplex capable
0	0	RO	Port 2 Link Partner 10 Half Duplex capability =1, link partner 10BT half duplex capable =0, link partner not 10BT half duplex capable

### 3.10.11 Ports 3 & 4 Auto Negotiation (AN) Register (SEP34AN Offset 0xE84C)

The following table shows the register bit fields. Default: 0x1F00\_1F00

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0		Reserved
30	0	RO	Port 3 AN complete. =1, AN done =0, AN not done
29	0	RW	Port 3 AN restart (self clearing). =1, restart auto-negotiation =0, normal operation
28	1	RW	Port 3 AN advertise flow control capability =1, advertise flow control capability =0, suppress flow control capability from transmission to link partner.
27	1	RW	Port 3 AN advertise 100 Full Duplex. =1, advertise 100BT Full duplex capability =0, suppress 100BT Full duplex capability from transmission to link





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			partner
26	1	RW	Port 3 AN advertise 100 Half Duplex. =1, advertise 100BT half duplex capability =0, suppress 100BT half duplex capability from transmission to link partner
25	1	RW	Port 3 AN advertise 10 Full Duplex. =1, advertise 10BT Full duplex capability =0, suppress 10BT Full duplex capability from transmission to link partner
24	1	RW	Port 3 AN advertise 10 Half Duplex. =1, advertise 10BT Half duplex capability =0, suppress 10BT Half duplex capability from transmission to link partner
23	0	RO	Port 3 Link status. =1, Link good =0, Link not good
22	0	RO	Port 3 duplex status (resolved).
21	0	RO	Port 3 speed status (resolved).
20	0	RO	Port 3 Link Partner flow Control capability =1, link partner flow control capable =0, link partner not flow control capable.
19	0	RO	Port 3 Link Partner 100 Full Duplex capability =1, link partner 100BT full duplex capable =0, link partner not 100BT full duplex capable
18	0	RO	Port 3 Link Partner 100 Half Duplex capability =1, link partner 100BT half duplex capable =0, link partner not 100BT half duplex capable
17	0	RO	Port 3 Link Partner 10 Full Duplex capability =1, link partner 10BT full duplex capable =0, link partner not 10BT full duplex capable
16	0	RO	Port 3 Link Partner 10 Half Duplex capability =1, link partner 10BT half duplex capable =0, link partner not 10BT half duplex capable
15	0		Reserved
14	0	RO	Port 4 AN complete. =1, AN done =0, AN not done
13	0	RW	Port 4 AN restart (self clearing). =1, restart auto-negotiation =0, normal operation
12	1	RW	Port 4 AN advertise flow control capability =1, advertise flow control capability =0, suppress flow control capability from transmission to link partner
11	1	RW	Port 4 AN advertise 100 Full Duplex. =1, advertise 100BT Full duplex capability =0, suppress 100BT Full duplex capability from transmission to link partner



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10	1	RW	Port 4 AN advertise 100 Half Duplex. =1, advertise 100BT half duplex capability =0, suppress 100BT half duplex capability from transmission to link partner
9	1	RW	Port 4 AN advertise 10 Full Duplex. =1, advertise 10BT Full duplex capability =0, suppress 10BT Full duplex capability from transmission to link partner
8	1	RW	Port 4 AN advertise 10 Half Duplex. =1, advertise 10BT Half duplex capability =0, suppress 10BT Half duplex capability from transmission to link partner
7	0	RO	Port 4 Link status. =1, Link good =0, Link not good
6	0	RO	Port 4 duplex status (resolved).
5	0	RO	Port 4 speed status (resolved).
4	0	RO	Port 4 Link Partner flow Control capability =1, link partner flow control capable =0, link partner not flow control capable.
3	0	RO	Port 4 Link Partner 100 Full Duplex capability =1, link partner 100BT full duplex capable =0, link partner not 100BT full duplex capable
2	0	RO	Port 4 Link Partner 100 Half Duplex capability =1, link partner 100BT half duplex capable =0, link partner not 100BT half duplex capable
1	0	RO	Port 4 Link Partner 10 Full Duplex capability =1, link partner 10BT full duplex capable =0, link partner not 10BT full duplex capable
0	0	RO	Port 4 Link Partner 10 Half Duplex capability =1, link partner 10BT half duplex capable =0, link partner not 10BT half duplex capable

### 3.10.12 Indirect Access Control Register (SEIAC Offset 0xE850)

The following table shows the register bit fields.

Note: a write will trigger a LUE command.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:13	0x00000	RO	Reserved
12	0	RW	Command read/write (self clearing): 1, read command 0, write command
11:10	00	RW	Table select: 00 = static mac address table selected 01 = VLAN table selected 10 = dynamic address table selected



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			11 = MIB counter selected 0
9:0	0x000	RW	Indirect address within the selected table

### 3.10.13 Indirect Access Data Register High 2 (SEIADH2 Offset 0xE854)

The following table shows the register bit fields.

Note: it is indirect, so the value written may not equal the value read.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:5	0x0		Reserved
4:0	-	RW	Bit 68-64 of indirect data

### 3.10.14 Indirect Access Data Register High 1 (SEIADH1 Offset 0xE858)

The following table shows the register bit fields. Default: 0x0000\_0000

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	-	RW	Bit 63-32 of indirect access data

### 3.10.15 Indirect Access Data Register Low (SEIADL Offset 0xE85C)

The following table shows the register bit fields. Default: 0x0000\_0000

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	-	RW	Bit 31-0 of indirect access data

### 3.10.16 Advance Feature Control Register (SEAFRC Offset 0xE860)

The following table shows the register bit fields. Default: 0x0000\_0000

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:27	0x00		Reserved
26:22	0x00	RW	Tag removal (msb = port 5, lsb= port 1). Bit 26, tag removal for internal LAN DMA port Bit 25, tag removal for port 4 Bit 24, tag removal for port 3 Bit 23, tag removal for port 2 Bit 22, tag removal for port 1  =1, when packets are output on the port, the switch will remove 802.1Q tags from packets with 802.1Q tags when received. The switch will not modify packets received without tags. =0, disable tag removal
21:17	0x00	RW	Tag insertion (msb = port 5, lsb= port 1) Bit 21, tag insertion for internal LAN DMA port Bit 20, tag insertion for port 4



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			<p>Bit 19, tag insertion for port 3 Bit 18, tag insertion for port 2 Bit 17, tag insertion for port 1</p> <p>=1, when packets are output on the port, the switch will add 802.1Q tags to packets without 802.1Q tags when received. The switch will not add tags to packets already tagged. The tag inserted is the ingress port's "port VID". =0, disable tag insertion</p>
16	0	RW	<p>Sniff mode select:</p> <p>1, AND – sniffer port will only look at packets that are received on the RX sniff port AND transmitted out from the TX sniff port (both source port and destination port need to match) 0, OR – sniffer port will look at packets that are received on the RX sniff port OR transmitted from the TX sniff port. (Either source port or destination port needs to match). This is the mode used to implement RX only sniff.</p>
15:11	0x00	RW	<p>Sniffer port select</p> <p>Bit 15, select internal LAN DMA port as sniffer port Bit 14, select port 4 as sniffer port Bit 13, select port 3 as sniffer port Bit 12, select port 2 as sniffer port Bit 11, select port 1 as sniffer port</p> <p>=1, Port is designated as sniffer port and will transmit packets that are monitored. =0, Port is a normal port</p>
10:6	0x00	RW	<p>TX mirror port select</p> <p>10, select internal LAN DMA port as TX mirror port 9, select port 4 as TX mirror port 8, select port 3 as TX mirror port 7, select port 2 as TX mirror port 6, select port 1 as TX mirror port</p> <p>=1, All the packets transmitted on the port will be marked as "monitored packets" and forwarded to the designated "sniffer port" =0, no transmit monitoring</p>
5:1	0x00	RW	<p>RX mirror port select</p> <p>5, select internal LAN DMA port as RX mirror port 4, select port 4 as RX mirror port 3, select port 3 as RX mirror port 2, select port 2 as RX mirror port 1, select port 1 as RX mirror port</p> <p>=1, All the packets received on the port will be marked as "monitored packets" and forwarded to the designated "sniffer port" =0, no receive monitoring</p>



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0	0	RW	IGMP snoop enable on Switch MII interface =1, IGMP snoop enabled. All the IGMP packets will be forwarded to Switch MII port. =0, IGMP snoop disabled.
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### 3.10.17 TOS Priority Register High (SEDSCPH Offset 0xE864)

The IPv4 TOS priority control registers implement a fully decoded 64 bit DSCP (Differentiated Services Code Point) register used to determine priority from the 6 bit TOS field in the IP header. The most significant 6 bits of the TOS field are fully decoded into 64 possibilities, and the singular code that results is compared against the corresponding bit in the DSCP register. If the register bit is a 1, the priority is high; if it is a 0, the priority is low.

The following table shows the register bit fields. Default: 0x0000\_0000

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	0x0	RW	DSCP [63:32]

### 3.10.18 TOS Priority Register Low (SEDSCPL Offset 0xE868)

The following table shows the register bit fields. Default: 0x0000\_0000

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	0x0	RW	DSCP [31:0]

### 3.10.19 Switch Engine MAC Address Register High (SEMAH Offset 0xE86C)

The following table shows the register bit fields. Default: 0x0000\_0010

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:16	0x0		Reserved
15:0	0x0010	RW	MAC address [47:32]

### 3.10.20 Switch Engine MAC Address Register Low (SEMAL Offset 0xE870)

The following table shows the register bit fields. Default: 0xA1FF\_FFFF

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	0xA1FF_FFFF	RW	MAC address [31:0]

### 3.10.21 LAN PHY Power Management Register for Ports 1 & 2 (LPPM12 Offset 0xE874)

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0	RO	Reserved



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30	0	RW	Port 1 PHY Loopback = 1, perform PHY loopback, ie. loopback MAC's RX back to TX. = 0, normal operation.
29	0	RW	Port 1 Remote Loopback = 1, perform remote loopback, ie. loopback PHY's RX back to TX. = 0, normal operation.
28	0	RW	Port 1 PHY Isolate = 1, electrical isolation of PHY from MII and TX+/TX- = 0, normal operation
27	0	RW	Port 1 PHY soft reset = 1, PHY soft reset = 0, normal operation
26	0	RW	Port 1 Force Link
25	0	RO	Port 1 MDIXS MDIX Status 1: MDIX 0: MDX
24	0	RO	Port 1 FEF Far End Fault 1: far end fault status detected 0: no far end fault status detected
23	0		Reserved
22	0	RW	Port 1 TXDIS Disable Port's Transmitter 1: disable port's transmitter 0: normal operation
21	0	RW	Port 1 DFEF Disable Far End Fault 1: disable far end fault detection & pattern transmission 0: enable far end fault detection & pattern transmission
20	0	RW	Port 1 PD Power Down 1: power down 0: normal operation
19	0	RW	Port 1 DMDX Disable Auto MDI/MDIX 1: disable auto MDI/MDIX function 0: enable auto MDI/MDIX function
18	0	RW	Port 1 FMDX Forced MDIX 1: if auto MDI/MDIX is disabled, force PHY into MDIX mode 0: do not force PHY into MDIX mode
17	0	RW	Port 1 MAC Loopback 1: perform "local loopback", i.e. loop back MAC's TX back to RX 0: normal operation
16:15	00	RO	Reserved
14	0	RW	Port 2 PHY Loopback = 1, perform PHY loopback, ie. loopback MAC's RX back to TX. = 0, normal operation.
13	0	RW	Port 2 Remote Loopback



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			= 1, perform remote loopback, ie. loopback PHY's RX back to TX. = 0, normal operation.
12	0	RW	Port 2 PHY Isolate = 1, electrical isolation of PHY from MII and TX+/TX- = 0, normal operation
11	0	RW	Port 2 PHY soft reset = 1, PHY soft reset = 0, normal operation
10	0	RW	Port 2 Force Link
9	0	RO	Port 2 MDIXS MDIX Status 1: MDIX 0: MDX
8	0	RO	Port 2 FEF Far End Fault 1: far end fault status detected 0: no far end fault status detected
7	0		Reserved
6	0	RW	Port 2 TXDIS Disable Port's Transmitter 1: disable port's transmitter 0: normal operation
5	0	RW	Port 2 DFEF Disable Far End Fault 1: disable far end fault detection & pattern transmission 0: enable far end fault detection & pattern transmission
4	0	RW	Port 2 PD Power Down 1: power down 0: normal operation
3	0	RW	Port 2 DMDX Disable Auto MDI/MDIX 1: disable auto MDI/MDIX function 0: enable auto MDI/MDIX function
2	0	RW	Port 2 FMDX Forced MDIX 1: if auto MDI/MDIX is disabled, force PHY into MDIX mode 0: do not force PHY into MDIX mode
1	0	RW	Port 2 MAC Loopback 1: perform "local loopback", i.e. loop back MAC's TX back to RX 0: normal operation
0	0		Reserved

### 3.10.22 LAN PHY Power Management Register for Ports 3 & 4 (LPPM34 Offset 0xE878)

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0	RO	Reserved
30	0	RW	Port 3 PHY Loopback = 1, perform PHY loopback, ie. loopback MAC's RX back to TX.





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			= 0, normal operation.
29	0	RW	Port 3 Remote Loopback = 1, perform remote loopback, ie. loopback PHY's RX back to TX. = 0, normal operation.
28	0	RW	Port 3 PHY Isolate = 1, electrical isolation of PHY from MII and TX+/TX- = 0, normal operation
27	0	RW	Port 3 PHY soft reset = 1, PHY soft reset = 0, normal operation
26	0	RW	Port 3 Force Link
25	0	RO	Port 3 MDIXS MDIX Status 1: MDIX 0: MDX
24	0	RO	Port 3 FEF Far End Fault 1: far end fault status detected 0: no far end fault status detected
23	0		Reserved
22	0	RW	Port 3 TXDIS Disable Port's Transmitter 1: disable port's transmitter 0: normal operation
21	0	RW	Port 3 DFEF Disable Far End Fault 1: disable far end fault detection & pattern transmission 0: enable far end fault detection & pattern transmission
20	0	RW	Port 3 PD Power Down 1: power down 0: normal operation
19	0	RW	Port 3 DMDX Disable Auto MDI/MDIX 1: disable auto MDI/MDIX function 0: enable auto MDI/MDIX function
18	0	RW	Port 3 FMDX Forced MDIX 1: if auto MDI/MDIX is disabled, force PHY into MDIX mode 0: do not force PHY into MDIX mode
17	0	RW	Port 3 MAC Loopback 1: perform "local loopback", i.e. loop back MAC's TX back to RX 0: normal operation
16:15	00		Reserved
14	0	RW	Port 4 PHY Loopback = 1, perform PHY loopback, ie. loopback MAC's RX back to TX. = 0, normal operation.
13	0	RW	Port 4 Remote Loopback = 1, perform remote loopback, ie. loopback PHY's RX back to TX. = 0, normal operation.



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12	0	RW	Port 4 PHY Isolate = 1, electrical isolation of PHY from MII and TX+/TX- = 0, normal operation
11	0	RW	Port 4 PHY soft reset = 1, PHY soft reset = 0, normal operation
10	0	RW	Port 4 Force Link
9	0	RO	Port 4 MDIXS MDIX Status 1: MDIX 0: MDX
8	0	RO	Port 4 FEF Far End Fault 1: far end fault status detected 0: no far end fault status detected
7	0		Reserved
6	0	RW	Port 4 TXDIS Disable Port's Transmitter 1: disable port's transmitter 0: normal operation
5	0	RW	Port 4 DFEF Disable Far End Fault 1: disable far end fault detection & pattern transmission 0: enable far end fault detection & pattern transmission
4	0	RW	Port 4 PD Power Down 1: power down 0: normal operation
3	0	RW	Port 4 DMDX Disable Auto MDI/MDIX 1: disable auto MDI/MDIX function 0: enable auto MDI/MDIX function
2	0	RW	Port 4 FMDX Forced MDIX 1: if auto MDI/MDIX is disabled, force PHY into MDIX mode 0: do not force PHY into MDIX mode
1	0	RW	Port 4 MAC Loopback 1: perform "local loopback", i.e. loop back MAC's TX back to RX 0: normal operation
0	0		Reserved

### 3.10.23 Static MAC address table

The switch built into the K8695P has both a static and a dynamic MAC address table. When a DA look up is requested, both tables will be searched to make a packet forwarding decision. When an SA look up is requested, only the dynamic table is searched for aging, migration and learning purposes. The static DA look up result will have precedence over the dynamic DA look up result. If there are DA matches in both tables, the result from the static table will be used. The entries in the static table will not be aged out by K8695P.

The lookup engine in the KS8695PX switch uses an absolute MAC address look up, meaning that it looks at all the bits in the MAC address to make packet forwarding decisions. This ensures that



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the switch will be able to forward any MAC address correctly. Other switches use a hashing table algorithm, which only looks at a subset of the bits in the MAC address to decide where to forward a packet. The result is that packets with similar MAC addresses may be dropped or forwarded incorrectly.

Note: Register bit assignments are different for static MAC table reads and static MAC table write as shown in the two tables below.

Format of static MAC table for reads (8 entries)

Bit	Name	R/W	Description	Default
60-57	FID	RO	Filter VLAN ID, representing one of the 16 active VLANs.	0000
56	Use FID	RO	=1, use (FID+MAC) to look up in static table =0, use MAC only to look up in static table	0
55	Reserved		Reserved	N/A
54	override	RO	=1, override spanning tree "transmit enable=0" or "receive enable=0" setting. This bit is used for spanning tree implementation =0, no override	0
53	valid	RO	=1, this entry is valid, the look up result will be used =0, this entry is not valid	0
52-48	Forwarding ports	RO	The 5 bits control the forward ports, ex 00001, forward to port 1 00010, forward to port 2 ..... 10000, forward to port 5 00110, forward to port 2 and port 3 11111, broadcasting (excluding the ingress port)	00000
47-0	MAC address	RO	48 bit mac address	0x0

Format of static MAC table for writes (8 entries)

Bit	Name	R/W	Description	Default
59-56	FID	W	Filter VLAN ID, representing one of the 16 active VLANs.	0000
55	Use FID	W	=1, use (FID+MAC) to look up in static table =0, use MAC only to look up in static table	0
54	override	W	=1, override spanning tree "transmit enable=0" or "receive enable=0" setting. This bit is used for spanning tree implementation =0, no override	0
53	valid	W	=1, this entry is valid, the look up result will be used =0, this entry is not valid	0
52-48	Forwarding ports	W	The 5 bits control the forward ports, ex 00001, forward to port 1 00010, forward to port 2 ..... 10000, forward to port 5 00110, forward to port 2 and port 3 11111, broadcasting (excluding the ingress port)	00000
47-0	MAC address	W	48 bit mac address	0x0



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Examples:

(1), Static Address Table Read (read the 2<sup>nd</sup> entry)

Write to SEIAC with 0x0000\_1001 (read, static table selected, and trigger the read operation)

Then

Read SEIADH1 (60-32)

Read SEIADL (31-0)

(2), Static Address Table Write (write the 8<sup>th</sup> entry)

Write SEIADH1 (59-32)

Write SEIADL (31-0)

Write to SEIAC with 0x0000\_0007 (write, static table selected, and trigger the write operation)

#### 3.10.24 VLAN table

VLAN table is used to do VLAN table look up. If 802.1Q VLAN mode is enabled (Register 5 bit 7 =1), this table will be used to retrieve VLAN information that the ingress packet is associated with. The information includes FID(filter ID), VID(VLAN ID), VLAN membership described below:

Format of static VLAN table (16 entries)

Bit	Name	R/W	Description	Default
21	Valid	R/W	=1, the entry is valid =0, entry is invalid	1
20-16	Membership	R/W	Specify which ports are members of the VLAN. If a DA look up fails (no match in both static and dynamic tables), the packet associated with this VLAN will be forwarded to ports specified in this field. Eg. 11001 means port 5,4, and 1 are in this VLAN.	11111
15-12	FID	R/W	Filter ID. K8695P supports 16 active VLANs represented by these four bit fields. FID is the mapped ID. If 802.1Q VLAN is enabled, the look up will be based on FID+DA and FID+SA.	0
11-0	VID	R/W	IEEE 802.1Q 12 bit VLAN ID	1

If 802.1Q VLAN mode is enabled, K8695P will assign a VID to every ingress packet. If the packet is untagged or tagged with a null VID, the packet is assigned with the default port VID of the ingress port. If the packet is tagged with non null VID, the VID in the tag will be used. The look up process will start from the VLAN table look up. If the VID is not valid, the packet will be dropped and no address learning will take place. If the VID is valid, the FID is retrieved. The FID+DA and FID+SA lookups are performed. The FID+DA look up determines the forwarding ports. If FID+DA fails, the packet will be broadcasted to all the members (excluding the ingress port) of the VLAN. If FID+SA fails, the FID+SA will be learned.

Examples:

(1), VLAN Table Read (read the 3<sup>rd</sup> entry)

Write to SEIAC with 0x0000\_1402 (read, VLAN table selected, and trigger the read operation)

Then

Read SEIADL (VLAN table bits 21-0)

(2), VLAN Table Write (write the 7<sup>th</sup> entry)

Write to SEIADL (VLAN table bits 21-0)

Write to SEIAC with 0x0000\_0406 (write, VLAN table selected, and trigger the write operation)



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#### 3.10.25 Dynamic MAC address table

This table is read only. The contents are maintained by K8695P only.  
Format of dynamic MAC address table (1K entries)

Bit	Name	R/W	Description	Default
68	MAC empty	RO	=1, there is no valid entry in the table =0, there are valid entries in the table	1
67-58	No of valid entries	RO	Indicates how many valid entries in the table 0x3ff means 1 K entries 0x1 means 2 entries 0x0 and bit 68 = 0: means 1 entry 0x0 and bit 68 = 1: means 0 entry	0
57-56	Time stamp	RO	2-bit counters for internal aging	
55	Data ready	RO	=1, The entry is not ready, retry until this bit is set to 0. =0, The entry is ready	
54-52	Source port	RO	The source port where FID+MAC is learned. 000 port 1 001 port 2 010 port 3 011 port 4 100 port 5	0x0
51-48	FID	RO	Filter ID	0x0
47-0	MAC address	RO	48 bit mac address	0x0

Examples:

(1), Dynamic MAC Address Table Read (read the 1<sup>st</sup> entry), and retrieve the MAC table size  
Write to SEIAC with 0x0000\_1800 (read, dynamic table selected, and trigger the read operation)

Then

Read SEIADH2 (68-64) // bits [68:56] show # of entries

Read SEIADH1 (63-32) // if bit [55] is 1, restart (reread) from this register

Read SEIADL (31-0)

(2), Dynamic MAC Address Table Read (read the 250<sup>th</sup> entry), without retrieving # of entries info  
Write to SEIAC with 0x0000\_1901 (read, dynamic table selected, and trigger the read operation)

Then

Read SEIADH1 (55-32) // if bit [55] is 1, restart (reread) from this register

Read SEIADL (31-0)

#### 3.10.26 MIB counters

The MIB counters are provided on per port basis. The indirect memory is as below:  
For port 1

**Table 3-Port 1 MIB Counter Indirect Memory Offsets**

Offset	Counter Name	Description
0x0	<b>RxLoPriorityByte</b>	Rx lo-priority (default) octet count including bad pkts
0x1	<b>RxHiPriorityByte</b>	Rx hi-priority octet count including bad pkts
0x2	<b>RxUndersizePkt</b>	Rx undersize pkts w/ good CRC



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0x3	<b>RxFragments</b>	Rx fragment pkts w/ bad CRC, symbol errors or alignment errors
0x4	<b>RxOversize</b>	Rx oversize pkts w/ good CRC (max: 1536 or 1522 bytes)
0x5	<b>RxJabbers</b>	Rx pkts longer than 1522B w/ either CRC errors, Alignment errors, or symbol errors. (Depends on max packet size setting).
0x6	<b>RxSymbolError</b>	Rx pkts w/ invalid data symbol and legal packet size.
0x7	<b>RxCRCError</b>	Rx pkts within (64,1522) bytes w/ an integral number of bytes and a bad CRC (Upper limit depends on max packet size setting).
0x8	<b>RxAlignmentError</b>	Rx pkts within (64,1522) bytes w/ a non-integral number of bytes and a bad CRC (Upper limit depends on max packet size setting).
0x9	<b>RxControl8808Pkts</b>	The number of MAC control frames received by a port with 88-08h in EtherType field.
0xA	<b>RxPausePkts</b>	The number of PAUSE frames received by a port. PAUSE frame is qualified with EtherType (88-08h), DA, control opcode (00-01), data length (64B min), and a valid CRC
0xB	<b>RxBroadcast</b>	Rx good broadcast pkts (not including errored broadcast pkts or valid multicast pkts)
0xC	<b>RxMulticast</b>	Rx good multicat pkts (not including MAC control frames, errored multicast pkts or valid broadcast pkts)
0xD	<b>RxUnicast</b>	Rx good unicast packets
0xE	<b>Rx64Octets</b>	Total Rx pkts (bad pkts included) that were 64 octets in length
0xF	<b>Rx65to127Octets</b>	Total Rx pkts (bad pkts included) that are between 65 and 127 octets in length
0x10	<b>Rx128to255Octets</b>	Total Rx pkts (bad pkts included) that are between 128 and 255 octets in length
0x11	<b>Rx256to511Octets</b>	Total Rx pkts (bad pkts included) that are between 256 and 511 octets in length
0x12	<b>Rx512to1023Octets</b>	Total Rx pkts (bad pkts included) that are between 512 and 1023 octets in length
0x13	<b>Rx1024to1522Octets</b>	Total Rx pkts (bad pkts included) that are between 1024 and 1522 octets in length (Upper limit depends on max packet size setting).
0x14	<b>TxLoPriorityByte</b>	Tx lo-priority good octet count, including PAUSE pkts
0x15	<b>TxHiPriorityByte</b>	Tx hi-priority good octet count, including PAUSE pkts
0x16	<b>TxLateCollision</b>	The number of times a collision is detected later than 512 bit-times into the Tx of a pkt
0x17	<b>TxPausePkts</b>	The number of PAUSE frames transmitted by a port
0x18	<b>TxBroadcastPkts</b>	Tx good broadcast pkts (not including errored broadcast or valid multicast pkts)
0x19	<b>TxMulticastPkts</b>	Tx good multicast pkts (not including errored multicast pkts or valid broadcast pkts)
0x1A	<b>TxUnicastPkts</b>	Tx good unicast pkts
0x1B	<b>TxDeferred</b>	Tx pkts by a port for which the 1st Tx attempt is delayed due to the busy medium
0x1C	<b>TxTotalCollision</b>	Tx total collision, half duplex only
0x1D	<b>TxExcessiveCollision</b>	A count of frames for which Tx fails due to excessive collisions
0x1E	<b>TxSingleCollision</b>	Successfully Tx frames on a port for which Tx is inhibited by exactly one collision
0x1F	<b>TxMultipleCollision</b>	Successfully Tx frames on a port for which Tx is inhibited by



## CENTAUR™ KS8695PX Register Description

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	more than one collision
--	-------------------------

For port 2, the base is 0x20, same offset definition (0x20-0x3f)

For port 3, the base is 0x40, same offset definition (0x40-0x5f)

For port 4, the base is 0x60, same offset definition (0x60-0x7f)

Format of Per Port MIB Counters (16 entries)

Bit	Name	R/W	Description	Default
31	Overflow	RO	=1, Counter overflow =0, No Counter overflow	0
30	Count Valid	RO	=1, Counter value is valid =0, Counter value is not valid	0
29-0	Counter values	RO	Counter value	0

**Table 4-All Port Dropped Packet MIB Counters**

Offset	Counter Name	Description
0x100	<b>Port1 TX Drop Packets</b>	Tx packets dropped due to lack of resources
0x101	<b>Port2 TX Drop Packets</b>	Tx packets dropped due to lack of resources
0x102	<b>Port3 TX Drop Packets</b>	Tx packets dropped due to lack of resources
0x103	<b>Port4 TX Drop Packets</b>	Tx packets dropped due to lack of resources
0x104	<b>LAN DMA TX Drop Packets</b>	Tx packets dropped due to lack of resources
0x105	<b>Port1 RX Drop Packets</b>	Rx packets dropped due to lack of resources
0x106	<b>Port2 RX Drop Packets</b>	Rx packets dropped due to lack of resources
0x107	<b>Port3 RX Drop Packets</b>	Rx packets dropped due to lack of resources
0x108	<b>Port4 RX Drop Packets</b>	Rx packets dropped due to lack of resources
0x109	<b>LAN DMA RX Drop Packets</b>	Rx packets dropped due to lack of resources

Format of All Port Dropped Packet MIB Counters

Bit	Name	R/W	Description	Default
30-16	Reserved	N/A	Reserved	N/A
15-0	Counter values	RO	Counter value	0

Note: All port dropped packet MIB counters do not indicate overflow or validity; therefore the application must keep track of overflow and valid conditions.

Examples:

(1), MIB counter read (read port 1 rx 64 counter)

Write to SEIAC with 0x0000\_1C0E (read, MIB counters selected, and trigger the read operation)

Then

Read SEIADL (counter value 31-0) // If bit 31 = 1, there was a counter overflow.

// If bit 30 = 0, restart (reread) from this register.

(2), MIB counter read (read port 2 rx 64 counter)

Write to SEIAC with 0x0000\_1C2E (read, MIB counter selected, and trigger the read operation)

Then

Read SEIADL (counter value 31-0) // If bit 31 = 1, there was a counter overflow.

// If bit 30 = 0, restart (reread) from this register.





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(3), MIB counter read (read port 1 tx drop packets)

Write to SEIAC with 0x0000\_1D00 (read, MIB counter selected, and trigger the read operation)

Then

Read SEIADL (counter value 15-0)

### NOTE:

(1) In the heaviest condition, the byte counter will overflow in 2 minutes. It is recommended that the software read all the counters at least every 30 seconds. The per port MIB counters are designed as “read clear”. A per port MIB counter will be cleared after it is accessed. All port dropped packet MIB counters are not cleared after they are accessed. The application needs to keep track of overflow and valid conditions on these counters.

## 3.11 Miscellaneous Registers

### 3.11.1 Device ID Register (DID Offset 0xEA00)

This read-only register holds a 16-bit Device ID.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:16	0x0	RO	Reserved
15:0	0x8695	RO	Device ID

### 3.11.2 Revision ID Register (RID Offset 0xEA04)

This register holds a 4-bit sub-device ID and a 4-bit Revision ID.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:8	0x0	RO	Reserved
7:4	0x1	RO	Sub-Device ID. Indicates this device is KS8695PX (PCI support).
3:0	0x1	RO	Revision ID

### 3.11.3 WAN Miscellaneous Control Register (WMC Offset 0xEA0C)

This register controls certain additional WAN port features not specified in the WAN DMA registers.

Main features are the in the physical coding sublayer (PCS) functionality.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	N/A	N/A	Reserved
30	0	RO	WANC WAN Auto-Negotiation Complete When set, it indicates the WAN port auto-negotiation has completed.
29	0	RW	WANR WAN Auto-Negotiation Restart Set to restart the WAN port PHY auto-negotiation process.



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28	1	RW	WANAP WAN Auto-Negotiation Advertise Pause
27	1	RW	WANA100F WAN Auto-Negotiation Advertise 100 Full Duplex
26	1	RW	WANA100H WAN Auto-Negotiation Advertise 100 Half Duplex
25	1	RW	WANA10F WAN Auto-Negotiation Advertise 10 Full Duplex
24	1	RW	WANA10H WAN Auto-Negotiation Advertise 10 Half Duplex
23	0	RO	WLS WAN Link Status
22	0	RO	WDS WAN Duplex Status (resolved)
21	0	RO	WSS WAN Speed Status (resolved)
20	0	RO	WLPP WAN Link Partner Pause
19	0	RO	WLP100F WAN Link Partner 100 Full Duplex
18	0	RO	WLP100H WAN Link Partner 100 Half Duplex
17	0	RO	WLP10F WAN Link Partner 10 Full Duplex
16	0	RO	WLP10H WAN Link Partner 10 Half Duplex
15	0	RW	WAND WAN Auto-Negotiation Disable
14	0	RW	WANF100 WAN Force 100 when Auto-Negotiation disabled
13	0	RW	WANFF WAN Force Full-Duplex when Auto-Negotiation disabled
12:7	0x00	RO	Reserved
6:4	000	RW	WLED1S WAN LED1 Select 000: Speed 001: Link 010: Full Duplex 011: Collision 100: TX/RX Activities 101: Full Duplex/ Collision 110: Link/ Activities
3	0	RO	Reserved
2:0	000	RW	WLED0S WAN LED0 Select 000: Speed 001: Link 010: Full Duplex 011: Collision 100: TX/RX Activities 101: Full Duplex/ Collision 110: Link/ Activities

### 3.11.4 WAN PHY Power Management Register (WPPM Offset 0xEA10)

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:15	0x0	RO	Reserved
		RW	WLPBK WAN Loopback



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14	0		1: perform "local loopback", i.e. loop back MAC's TX back to RX 0: normal operation
13	0	RW	WRLPBK WAN Remote Loopback 1: perform remote loopback, ie. loopback PHY's RX back to TX. 0: normal operation.
12	0	RW	WPI WAN PHY Isolate 1: electrical isolation of PHY from MII and TX+/TX- 0: normal operation
11	0	RO	Reserved
10	0	RW	WFL WAN Force Link 1: force link in the PHY 0: normal operation
9	0	RO	MDIXS MDIX Status 1: MDIX 0: MDX
8	0	RO	FEF Far End Fault 1: far end fault status detected 0: no far end fault status detected
7	0	RW	AMDIXP Auto MDIX Parameter 1: don't follow IEEE specification for auto-negotiation 0: follow IEEE specification for auto-negotiation
6	0	RW	TXDIS Disable Port's Transmitter 1: disable port's transmitter 0: normal operation
5	0	RW	DFFEF Disable Far End Fault 1: disable far end fault detection & pattern transmission 0: enable far end fault detection & pattern transmission
4	0	RW	PD Power Down 1: power down 0: normal operation
3	0	RW	DMDX Disable Auto MDI/MDIX 1: disable auto MDI/MDIX function 0: enable auto MDI/MDIX function
2	0	RW	FMDX Forced MDIX 1: if auto MDI/MDIX is disabled, force PHY into MDIX mode 0: do not force PHY into MDIX mode
1	0	RW	LPBK MAC Loopback 1: perform "local loopback", i.e. loop back MAC's TX back to RX 0: normal operation
0	0	RO	Reserved

### 3.11.5 PHY Power Save Register (PPS Offset 0xEA1C)

The following table shows the register bit fields.



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BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:1	0x0	RO	Reserved
0	0	RO	PPSM PHY Power Save Mode 1: Enable PHY power save mode 0: Disable PHY power save mode

### 4.0 Host Communication

This chapter describes the descriptor lists and data buffers, which are collectively called the host communication area, that manage the actions and status related to buffer management. Commands and signals that control the functional operation of the KS8695PX are also described. The KS8695PX and the driver communicate through the two data structures: System Configuration registers (SCRs) and Descriptor Lists and Data Buffers.

Note: All unused bits the data structure in this chapter are reserved and should be written by the driver as zero.

#### 4.1 Descriptor Lists and Data buffers

The KS8695PX transfers received data frames to the receive buffer in host memory and transmits data from the transmit buffers in host memory. Descriptors that reside in the host memory act as pointers to these buffers.

There are two descriptor lists, one for receive and one for transmit for each MAC DMA(WAN and LAN). The base address of each list for WAN is written on WTDLB, and WRDLB, respectively. The base address of each list for LAN is written on LTDLB, and LRDLB, respectively. A descriptor list is forward linked. The last descriptor may point back to the first entry to create a ring structure. Descriptors are chained by setting the *next address* to next buffer in both the receive and transmit descriptors.

The descriptor lists reside in the host *physical* memory address space. Each pointer points to one buffer and the second pointer points to the next descriptor. This enables the greatest flexibility for the host to chain any data buffers with discontinuous memory location. This eliminates processor-intensive tasks such as memory copying from the host to memory.

A data buffer contains of either an entire frame or part of a frame, but it cannot exceed a single frame. Buffers contain only data; buffer status is maintained in the descriptor. Data chaining refers to frames that span multiple data buffers. Data chaining can be enabled or disabled. Data buffers reside in host physical memory space.

The descriptor structures for WAN and LAN are identical. For simplicity, they are both collectively referred to as RDES0-3, and TDES0-3 for receive and transmit.

#### 4.2 Receive Descriptors (RDES0-RDES3)

Receive descriptors and buffers addresses must be Word aligned. Each receive descriptor provides one frame buffer, one byte count field, as well as control and status bits.

The following table shows the RDES0 register bit fields.

BITS FIELD	DESCRIPTION
31	OWN Own Bit When set, indicates that the descriptor is owned by the KS8695PX. When



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	reset, indicates that the descriptor is owned by the host. The KS8695PX clears this bit either when it completes the frame reception or when the buffers that are associated with this descriptor are full.
30	FS First Descriptor When set, indicates that this descriptor contains the first buffer of a frame. If the buffer size of the first buffer is 0, the next buffer contains the beginning of the frame.
29	LS Last Descriptor When set, indicates that the buffer pointed by this descriptor is the last buffer of the frame.
28	IPE IP Checksum Error When set, indicates that the received frame is an IP packet and its IP checksum field does not match. This bit is valid only when last descriptor is set.
27	TCPE TCP Checksum Error When set, indicates that the received frame is an TCP/IP packet and its TCP checksum field does not match. This bit is valid only when last descriptor is set.
26	UDPE UDP Checksum Error When set, indicates that the received frame is an UDP/IP packet and its UDP checksum field does not match. This bit is valid only when last descriptor is set.
25	ES Error Summary Indicates the logical OR of the following RDES0 bits: CRC error Frame too long Runt frame This bit is valid only when last descriptor is set.
24	MF Multicast Frame When set, indicates that this frame has a multicast address. This bit is valid only when last descriptor is set.
23:20	Reserved
19	RE Report on MII Error When set, indicates that a receive error in the physical layer was reported during the frame reception.
18	TL Frame Too Long When set, indicates that the frame length exceeds the maximum size of 1518 bytes. This bit is valid only when last descriptor is set. Note: Frame too long is only a frame length indication and does not cause any frame truncation.
17	RF Runt Frame When set, indicates that this frame was damaged by a collision or premature termination before the collision window has passed. Runt frames are passed on the host only if the pass bad frames bit is set.
16	CE CRC Error



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	Wen set, indicates that a CRC error occurred on the received frame. This bit is valid only when last descriptor is set.
15	FT Frame Type When set, indicates that the frame is an Ethernet-type frame (frame length field is greater than 1500 bytes). When clear, indicates that the frame is an IEEE 802.3 frame. This bit is not valid for runt frames. This bit is valid only when last descriptor is set.
14:11	Reserved
10:0	FL Frame Length Indicates the length, in bytes, of the received frame, including the CRC. This field is valid only when last descriptor is set and descriptor error is reset.

The following table shows the RDES1 register bit fields.

BIT FIELD	DESCRIPTION
31:26	Reserved
25	RER Receive End of Ring When set, indicates that the descriptor list reached its final descriptor. The KS8695PX returns to the base address of the list, thus creating a descriptor ring.
24:12	Reserved
10:0	RBS Receive Buffer Size Indicates the size, in bytes, of the receive data buffer. If the field is 0, the KS8695PX ignores this buffer and moves to the next descriptor. The buffer size must be a multiple of 4.

The following table shows the RDES2 register bit fields.

BIT FIELD	DESCRIPTION
31:0	Buffer Address Indicates the physical memory address of the buffer. The buffer address must be Word aligned.

The following table shows the RDES3 register bit fields.

BIT FIELD	DESCRIPTION
31:0	Next Descriptor Address Indicates the physical memory address of the next descriptor in the descriptor ring. The buffer address must be Word aligned.

### 4.3 Transmit Descriptors (TDES0-TDES3)

Transmit descriptors must be Word aligned. Each descriptor provides one frame buffer, one byte count field, as well as control and status bits.

The following table shows the TDES0 register bit fields.

BIT FIELD	DESCRIPTION
-----------	-------------



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31	<p>OWN Own Bit</p> <p>When set, indicates that the descriptor is owned by the KS8695PX. When cleared, indicates that the descriptor is owned by the host. The KS8695PX clears this bit either when it completes the frame transmission or when the buffer allocated in the descriptor is empty.</p> <p>The ownership bit of the first descriptor of the frame should be set after all subsequent descriptors belonging to the same frame have been set. This avoids a possible race condition between the KS8695PX fetching a descriptor and the driver setting an ownership bit.</p>
30:0	Reserved

The following table shows the TDES1 register bit fields.

BIT FIELD	DESCRIPTION
31	<p>IC Interrupt on Completion</p> <p>When set, the KS8695PX set transmit interrupt after the present frame has been transmitted. It is valid only when last segment is set.</p>
30	<p>FS First Segment</p> <p>When set, indicates that the buffer contains the first segment of a frame.</p>
29	<p>LS Last Segment</p> <p>When set, indicates that the buffer contains the last segment of a frame.</p>
28	<p>IPCKG IP Checksum Generate</p> <p>When set, the KS8695PX will generate correct IP checksum for outgoing frames that contains IP protocol header. The KS8695PX supports only standard IP header, i.e. IP with 20 byte header. When this feature is used, ADD CRC bit in the transmit mode register should always be set.</p> <p>This bit is used as a per-packet control when the IP checksum generate bit in the transmit mode register is not set.</p> <p>This bit should be always set for multiple-segment packets.</p>
27	<p>TCPCKG TCP Checksum Generate</p> <p>When set, the KS8695PX will generate correct TCP checksum for outgoing frames that contains IP and TCP protocol header. The KS8695PX supports only standard IP header, i.e. IP with 20 byte header. When this feature is used, ADD CRC bit in the transmit mode register should always be set.</p> <p>This bit is used as a per-packet control when the TCP checksum generate bit in the transmit mode register is not set.</p> <p>This bit should be always set for multiple-segment packets.</p>
26	<p>UDPCKG UDP Checksum Generate</p> <p>When set, the KS8695PX will generate correct UDP checksum for outgoing frames that contains IP and UDP protocol header. The KS8695PX supports only standard IP header, i.e. IP with 20 byte header. When this feature is used, ADD CRC bit in the transmit mode register should always be set.</p> <p>This bit is used as a per-packet control when the UDP checksum generate bit in the transmit mode register is not set.</p>
25	<p>TER Transmit End of Ring</p> <p>When set, indicates that the descriptor pointer has reached its final descriptor.</p> <p>The KS8695PX returns to the base address of the list, forming a descriptor</p>





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	ring.
24	Reserved
23:11	Reserved
10:0	TBS Transmit Buffer Size Indicates the size, in bytes, of the transmit data buffer. If this field is 0, the KS8695PX ignores this buffer and moves to the next descriptor.

The following table shows the TDES2 register bit fields.

BIT FIELD	DESCRIPTION
31:0	Buffer Address Indicates the physical memory address of the buffer. There is no limitation on the transmit buffer address alignment.

The following table shows the TDES3 register bit fields.

BIT FIELD	DESCRIPTION
31:0	Next Descriptor Address Indicates the physical memory address of the next descriptor in the descriptor ring. The buffer address must be Word aligned.



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### 4.4 Contact Information

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## CENTAUR™ KS8695PX Register Description

Integrated Multi-Port PCI Gateway Solution

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